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(54) Title: ELECTROLUMINESCENT LAMINATE WITH THICK FILM DIELECTRIC

(57) Abstract

An improved dielectric layer of an electroluminescent laminate, and method of preparation are provided. The dielectric layer is formed as a thick layer from a ceramic material to provide: a dielectric strength greater than about 1.0×10^6 V/m; a dielectric constant such that the ratio of the dielectric constant of the dielectric material to that of the phosphor layer is greater than about 50:1; a thickness such that the ratio of the thickness of the dielectric layer to that of the phosphor layer is in the range of about 20:1 to 500:1; and a surface adjacent the phosphor layer which is compatible with the phosphor layer and sufficiently smooth that the phosphor layer illuminates generally uniformly at a given excitation voltage. The invention also provides for electrical connection of an electroluminescent laminate to voltage driving circuitry with through hole technology. The invention also extends to laser scribing the transparent conductor lines of an electroluminescent laminate.

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1 **ELECTROLUMINESCENT LAMINATE WITH THICK FILM DIELECTRIC**
2 FIELD OF THE INVENTION

3 This invention relates to electroluminescent
4 laminates and methods of manufacturing same. The invention
5 also relates to electroluminescent display panels providing
6 for electrical connection from the electroluminescent
7 laminate to voltage driving circuitry. The invention
8 further relates to laser scribing a pattern in a planar
9 laminate such as the address lines of the transparent
10 electrode of an electroluminescent laminate.

11 **BACKGROUND OF THE INVENTION**

12 Electroluminescence (EL) is the emission of light
13 from a phosphor due to the application of an electric field.
14 Electroluminescent devices have utility as lamps and
15 displays. Currently, electroluminescent devices are used in
16 flat panel display systems, involving either pre-defined
17 character shapes or individually addressable pixels in a
18 rectangular matrix.

19 Pioneering work in electroluminescence was done at
20 GTE Sylvania. An AC voltage was applied to powder or
21 dispersion type EL devices in which a light emitting
22 phosphor powder was imbedded in an organic binder deposited
23 on a glass substrate and covered with a transparent
24 electrode. These powder or dispersion type EL devices are
25 generally characterized by low brightness and other problems
26 which have prevented widespread use.

27 Thin film electroluminescent (TFEL) devices were
28 developed in the 1950's. The basic structure of an AC
29 thin layer EL laminate is well known, see for example
30 Tornqvist, R.O. "Thin-Film Electroluminescent Displays",
31 Society for Information Display, 1989, International
32 Symposium Seminar Lecture Notes, and U.S. Patent
33 4,857,802 to Fuyama et al. A phosphor layer is sandwiched
34 between a pair of electrodes and separated from the
35 electrodes by respective insulating/dielectric

1 layers. Most commonly, the phosphor material is ZnS
2 with Mn included as an activator (dopant). The ZnS:Mn
3 TFEL is yellow emitting. Other colour phosphors have
4 been developed.

5 The layers of conventional TFEL laminates are
6 deposited on a substrate, usually glass. Deposition of
7 the layers is done sequentially by known thin film
8 techniques, for example electron beam (EB) vacuum
9 evaporation or sputtering and, more recently, by atomic
10 layer epitaxy (ALE). The thickness of the entire TFEL
11 laminate is only in the order of one or two microns.

12 To separate and electrically insulate the
13 phosphor layer from the electrodes, various
14 insulating/dielectric materials are known and used, as
15 discussed in more detail hereinafter.

16 Each of the two electrodes differ, depending
17 on whether it is at the "rear" or the "front" (viewing)
18 side of the device. A reflective metal, such as
19 aluminum is typically used for the rear electrode. A
20 relatively thin optically transmissive layer of indium
21 tin oxide (ITO) is typically employed as the front
22 electrode. In lamp applications, both electrodes take
23 the form of continuous layers, thereby subjecting the
24 entire phosphor layer between the electrodes to the
25 electric field. In a typical display application, the
26 front and rear electrodes are suitably patterned with
27 electrically conductive address lines defining row and
28 column electrodes. Pixels are defined where the row and
29 column electrodes overlay. Various electronic display
30 drivers are well known which address individual pixels
31 by energizing one row electrode and one column electrode
32 at a time.

33 While simple in concept, the development of
34 thin film electroluminescent devices has met with many
35 practical difficulties. A first difficulty arises from
36 the fact that the devices are formed from individual
37 laminate layers deposited by thin film techniques which

1 are time consuming and costly techniques. A very small
2 defect in any particular layer can cause a failure.
3 Secondly, these thin-film devices are typically operated
4 at relatively high voltages, eg. 300 - 450 volts peak to
5 peak. In fact, these voltages are such that the
6 phosphor layer is operated beyond its dielectric
7 breakdown voltage, causing it to conduct. The thin-film
8 dielectric layers on either side of the phosphor layer
9 are required to limit or prevent conduction between the
10 electrodes. The application of the large electric
11 fields can cause electrical breakdown between the
12 electrodes, resulting in failure of the device.

13 The present invention is particularly directed
14 to the insulating/dielectric layers of
15 electroluminescent devices and the prevention of
16 electrical discharges across the phosphor layer. A
17 requirement for successful operation of an
18 electroluminescent device is that the electrodes
19 (address lines) be electrically isolated from the
20 phosphor layer. This function is provided by the
21 insulating/dielectric layers. Typically,
22 insulating/dielectric layers are provided on either side
23 of the phosphor layer and are constructed from alumina,
24 yttria, silica, silicon nitride or other dielectric
25 materials. During operation of the device, electrons
26 from the interface between the insulating layer and the
27 phosphor layer are accelerated by the electric field as
28 they pass through the phosphor layer, and collide with
29 the dopant atoms in the phosphor layer, emitting light
30 as a result of the collision process. In a conventional
31 TFEL device, to ensure that the electric field strength
32 across the phosphor is sufficiently high, the thickness
33 of the dielectric layers is usually kept less than or
34 comparable to that of the phosphor layer. If the
35 dielectric layers are too thick a large portion of the
36 voltage applied between the address lines is across the
37 dielectric layers rather than across the phosphor layer.

1 It is important that the dielectric material
2 be compatible with the phosphor layer. By "compatible",
3 as used in this specification and in the claims, is
4 meant that, firstly, it provides a good injectivity
5 interface, i.e. a source of "hot" electrons at the
6 phosphor interface which can be promoted or tunnelled
7 into the phosphor conduction band to initiate conduction
8 and light emission in the phosphor layer on application
9 of an electric field. Secondly, within the meaning of
10 compatible, the dielectric material must be chemically
11 stable so that it does not react with adjacent layers,
12 that is the phosphor or the electrodes.

13 In a typical TFEL, in order to achieve
14 sufficient luminosity, the applied voltage is very near
15 that at which electrical breakdown of the dielectric
16 occurs. Thus, the manufacturing control over the
17 thickness and quality of the dielectric and phosphor
18 layers must be stringently controlled to prevent
19 electrical breakdown. This requirement in turn makes it
20 difficult to achieve high manufacturing yields.

21 A typical TFEL structure is constructed from
22 the front (viewing) side to the rear. The thin layers
23 are sequentially deposited on a suitable substrate.
24 Glass substrates are utilized to provide transparency.
25 The transparent, front electrode (ITO address lines) is
26 deposited on the glass substrate by sputtering to a
27 thickness of about 0.2 microns. The subsequent
28 dielectric - phosphor - dielectric layers are then
29 usually deposited by sputtering or evaporation. The
30 thickness of the phosphor layer is typically about 0.5
31 microns. The dielectric layers are typically about 0.4
32 microns thick. The phosphor layer is usually annealed
33 after deposition at about 450°C to improve efficiency.
34 The rear electrode is then added, typically in the form
35 of aluminum address lines with a thickness of 0.1
36 microns. The finished TFEL laminate is encapsulated in
37 order to protect it from external humidity. Epoxy

laminated cover glass or silicon oil encapsulation are used. In that the initial substrate used for deposition is typically glass, the materials and deposition techniques employed in TFEL laminate construction cannot demand high temperature processing.

The high electric field strength used to operate a TFEL device puts heavy requirements on the dielectric layers. High dielectric strengths are required to avoid electrical breakdown. Dielectrics with high dielectric constants are preferred in order to provide luminosity at the lowest possible driving voltage. However, efforts to utilize high dielectric constant materials have not provided satisfactory results.

To lower the driving voltage of TFEL elements insulating layers have been constructed from higher dielectric constant materials, for instance SrTiO₃, PbTiO₃, and BaTa₂O₅, as reported in U.S. Patent 4,857,802 issued to Fuyama et al. However, these materials have not performed well, exhibiting low dielectric breakdown strengths. In U.S. Patent 4,857,802, a dielectric layer is formed from a perovskite crystal structure by controlled thin film deposition techniques to achieve an increased (111) plane orientation. The patent reports increased dielectric strengths (above about 8.0×10^5 - about 1.0×10^6 V/cm) with a dielectric layer having a thickness of about 0.5 microns using SrTiO₃, PbTiO₃, and BaTiO₃, all of which have high dielectric constants and a perovskite crystal structure. This device still has the disadvantage of requiring complex and difficult to control thin film deposition techniques for the dielectric layer.

Efforts have also been made to develop TFEL devices using a thick ceramic insulator layer and a thin film electroluminescent layer, see Miyata, T. et al., SID 91 Digest, pp 70-73 and 286-289. The device is built up from a BaTiO_3 ceramic sheet. The sheet is

1 formed by molding fine BaTiO₃ powder into disks (20 mm
2 diameter) by conventional cold-press methods. The disks
3 are sintered in air at 1300°C, then ground and polished
4 into sheets with a thickness of about 0.2 mm. The
5 emitting layer is deposited onto the sheet in a thin
6 film using chemical vapour deposition or RF magnetron
7 sputtering. Suitable electrode layers are then
8 deposited by thin film techniques on either side of the
9 structure. While this device exhibits certain desirable
10 characteristics, it is not feasible to manufacture a
11 commercial TFEL device from a solid ceramic sheet.
12 Grinding and polishing a larger ceramic sheet to a
13 consistent thickness of 0.2 mm is not practical
14 economically.

15 It is also known in the art to use multiple
16 insulating/dielectric layers on each side of the
17 phosphor layer. For instance, U.S. Patent 4,897,319 to
18 Sun discloses a TFEL with an EL phosphor layer
19 sandwiched between a pair of insulator stacks, in which
20 one or both of the insulator stacks includes a first
21 layer of silicon oxynitride (SiON) and a second thicker
22 layer of barium tantalate (BTO). The first, SiON layer
23 provides high resistivity while the second, BTO layer
24 has a higher dielectric constant. Overall, the
25 structure is stated to produce a higher luminance of the
26 phosphor layer at conventional voltages. However, the
27 insulating layers are deposited by RF sputtering, which
28 has the disadvantages of thin film techniques described
29 hereinabove.

30 There is a need for a TFEL device having
31 higher luminosity and lower operating voltage than
32 conventional TFEL devices, while still being feasible to
33 construct. It is necessary to achieve this with a
34 dielectric layer which has a dielectric strength that is
35 above the electric field strength needed to drive the
36 device.

1 Fabricating electrode patterns in transparent
2 conductor materials such as indium tin oxide often
3 involves extensive and expensive masking,
4 photolithographic and chemical etching processes.
5 Lasers have been proposed for scribing such transparent
6 conductor materials. Generally carbon dioxide, argon
7 and YAG lasers are used. Such lasers produce light in
8 the visible and infrared ranges of the electromagnetic
9 spectrum (generally greater than 400 nm). However,
10 there are problems in using such long wavelength light
11 to scribe electrode patterns, particularly when the
12 transparent conductor material is deposited on another
13 transparent layer. In conventional TFEL displays, the
14 transparent electrode material, typically indium tin
15 oxide (ITO), is deposited on the transparent display
16 glass (substrate) prior to depositing the remaining
17 layers of the EL laminate. In an insulator or a
18 semiconducting material, light with a wavelength longer
19 than that corresponding to the energy of the electronic
20 band gap in the material is not strongly absorbed. For
21 optically transparent materials, the wavelength
22 corresponding to the band gap is shorter than that for
23 visible light. Therefore, transparent electrode
24 materials show poor absorption of laser light due to
25 both the long wavelength of the light and the thinness
26 of the layer, making it difficult to utilize laser
27 energy to directly ablate the electrode address lines.

28 U.S. Patents 4,292,092, to Hanak and
29 4,667,058, to Catalano et al., disclose processes to
30 pattern a transparent electrode pattern deposited on
31 another transparent layer in a solar battery. The
32 patents teach patterning the electrode using a pulsed
33 YAG laser, which produces light with a wavelength too
34 long to be significantly absorbed in any of the
35 transparent layers. To compensate for the low
36 absorption, a laser with high peak power is used to
37 thermally vaporize the transparent electrode. A

1 neodymium YAG laser is operated at 4-5 W with a pulse
2 rate of 36 KHz at a scanning rate of 20 cm/sec. The
3 examples of the patent disclose scribing an ITO layer
4 deposited on glass in this manner. However, the scribed
5 lines are described as having incompletely removed the
6 ITO and, in places, as having melted the glass to a
7 depth of a few hundred angstroms. The residual ITO must
8 thereafter be removed by a subsequent etching step.

9 Other approaches to forming electrode patterns
10 in transparent electrode materials involve using an
11 excimer laser, which produces light of shorter
12 wavelength, in the ultraviolet region of the
13 electromagnetic spectrum. At this wavelength, the laser
14 energy can be absorbed by the transparent electrode
15 material. Lasers of this nature are suggested to form
16 conductive patterns for liquid crystal displays (U.S.
17 Patents 4,980,366, to Imatou et al and 4,927,493, to
18 Yamazaki et al.), photovoltaic batteries (U.S. Patents
19 4,783,421, to Carlson et al. and 4,854,974, to Yamazaki
20 et al.) imaging sensors (U.S. Patent 5,043,567, to
21 Sakama et al.), and integrated circuits (U.S. Patent
22 5,109,149, to Leung). WO 90/0970, published August 23,
23 1990, to Autodisplay A/S, discloses a process for
24 scribing an electrode dot matrix pattern in a
25 transparent conductor on a transparent substrate with an
26 excimer laser.

27 While excimer lasers produce light which has
28 a wavelength short enough to be absorbed by the
29 transparent electrode such that the electrode may be
30 patterned by direct ablation, such lasers are relatively
31 expensive and the scribing process must be carefully
32 controlled to avoid melting or ablating the underlying
33 display glass. Furthermore, such processes may lead to
34 excessive or incomplete ablation of the transparent
35 electrode material. For instance in WO 90/0970 there is
36 an indication that, in the event of partial removal of

1 the material to be ablated, remaining portions may be
2 removed by chemicals or plasma etching.

3 Another problem encountered in scribing
4 transparent electrode materials on a transparent
5 substrate is addressed in U.S. patent 4,937,129, to
6 Yamazaki. To avoid diffusion or cross contamination
7 between the layers, diffusion barrier layers are
8 provided at the interface.

9 Other patents have taught surface treatments
10 of the transparent electrode material to enhance
11 absorption of the laser light. For instance, U.S.
12 Patent 4,909,895, to Cusano, teaches oxidizing the
13 metallic film surface to make it less reflective of the
14 laser light. U.S. Patent 4,568,409, to Caplan, teaches
15 coating the transparent layer to be ablated with a dye
16 to selectively absorb laser light where ablation is
17 desired.

18 Control circuitry to drive an EL display has
19 been developed. Basically, the circuitry converts
20 serial video data into parallel data to apply a voltage
21 to the rows and columns of the display. State of the
22 art row and column driver components (chips) are
23 available.

24 Asymmetric and symmetric drive techniques are
25 used with EL displays. In an asymmetric drive method,
26 the EL panel is provided with drive pulses by applying
27 a negative subthreshold voltage to one row at a time.
28 During each row scan time, a positive voltage pulse is
29 applied to the selected columns (i.e. those that should
30 illuminate) and zero voltage is applied to the
31 nonselected columns (i.e. those that should not
32 illuminate). At the intersection of selected columns
33 and rows, a voltage equal to the sum of the subthreshold
34 row voltage and the positive pulse voltage on the column
35 is applied across the pixel, causing light emission.
36 After all rows of the panel have been addressed, a

1 positive polarity refresh pulse is applied to all of the
2 rows simultaneously, and all columns are held at 0 V.

3 In a symmetrical drive scheme, the refresh
4 pulse is eliminated. Instead, a similar set of drive
5 pulses that are of the opposite polarity are applied to
6 the panel. To maintain the panel in operation, the rows
7 are scanned with pulses of alternating polarity on even
8 and odd frames. The alternating polarity produces a net
9 zero charge on all display pixels.

10 State of the art high voltage driver
11 components (chips) are available for both asymmetric and
12 symmetric drive techniques.

13 Alternate driving circuits and components for
14 EL displays are known or are in development, see for
15 example K. Shoji et al, Bidirectional Push-Pull
16 Symmetric Driving Method of TFEL Display, Springer
17 Proceedings in Physics, Vol. 38, 1989, 324; and Sutton
18 S. et al, Recent Developments and Trends in Thin-Film
19 Electroluminescent Display Drivers, Springer Proceedings
20 in Physics, Vol. 38, 1989, 318; and Bolger et al, A
21 Second Generation Chip Set for Driving EL Panels, SID,
22 1985, 229.

23 The above driving schemes are termed
24 multiplexed (passive) matrix addressing schemes.
25 Theoretically, other types of driving schemes, such as
26 active matrix addressing schemes, could be used with EL
27 displays. However, these are not yet developed. Such
28 alternate driving schemes should be considered to be
29 within the meaning of the phrase voltage driving
30 circuitry as used in this application.

31 In conventional EL displays, one method to
32 connect the column and row address lines to the driver
33 circuit is to compress a polymeric strip containing very
34 many closely spaced metal sheets between rows of
35 contacts connected to the display address lines and rows
36 of contacts connected to the driver components of the
37 driver circuit, which is constructed on a separate

1 circuit board (see U.S. Patent 4,508,990, to Essinger).
2 The polymeric strip is a layered elastomeric element
3 (LEE), known by such tradenames as STAX and ZEBRA. The
4 LEE is composed of alternating layers of conductive and
5 non-conductive elastomeric materials. The polymeric
6 strip avoids the need to laboriously connect hundreds of
7 individual wires using solder or welded connections to
8 the contacts. However, this interconnection technology
9 is unreliable, and does not function well at high
10 temperatures, which can cause the polymeric material to
11 creep.

12 Another method that is commonly used to
13 connect column and row address lines to the driver
14 circuit for liquid crystal displays (LCDs) is being
15 considered for electroluminescent displays, namely chip-
16 on-glass (COG) technology. The driver components
17 (chips) to which the address lines must be connected are
18 mounted around the periphery of the display. In the
19 case of LCDs, the address lines, which are evaporated on
20 the rear side of the display glass, are extended from
21 the active region of the display so that they end in
22 contact pads that are arranged in a pattern so that the
23 chips can be wire bonded thereto. Wire bonding entails
24 mounting the chips on the display glass and then
25 individually welding fine gold wires to the output pads
26 on the chip and to the corresponding contact pads on the
27 address lines.

28 The advantage of COG technology is that the
29 number of contacts between the display glass and the
30 driver circuit are substantially reduced, since by far
31 the largest number of contacts are between the driver
32 chips and the address lines. There are typically only
33 about 20 to 30 connections between the driver chips and
34 the rest of the driving circuit as opposed to up to 2000
35 connections to the address lines.

36 One major disadvantage of the COG technology
37 is that difficulty is experienced in wire bonding the

1 driver chips to connect them to the thin film pads on
2 the address lines, resulting in poor manufacturing
3 yields. Another disadvantage is that space is required
4 around the perimeter of the display to mount the driver
5 chips, thus increasing the bulkiness of the displays and
6 eliminating any possibility of joining several display
7 modules in an array to form a larger display.

7 modules in an array.

8 Through hole technology for direct circuit

9 connections is widely known in the semiconductor art

10 (see for example U.S Patent 3,641,390, Nakamura). U.S.

11 Patent 4,710,395, to Young et al, describes methods and

12 apparatus for through hole substrate printing with

13 regulated vacuum. However, through hole printing has

14 not, to the inventors' knowledge, been successfully

15 applied to EL displays.

U.S. Patent 3,504,214 to Lake et al describes a segmented storage type of EL device in which pixels are turned on with light to make a photoconductive layer next to the phosphor layer become electrically conductive. Complex through hole conductors are described. The patent indicates that ordinary through hole connections do not work with high resolution TFEL displays because the conductive material might react with the phosphor, thereby degrading the performance of the display.

SUMMARY OF THE INVENTION

Layers of a electroluminescent laminate have different dielectric constants. A potential difference across the layers of the laminate is divided proportionately across each layer in accordance with the thickness of each layer, and inversely with the relative dielectric constants of the materials. For instance, if one layer has a thickness and a dielectric constant that are both twice that of the other layer, the voltage would be divided equally between the two layers. The present invention uses this property to combine a thick

1 dielectric layer having a high dielectric constant with
2 a thinner phosphor layer having a substantially lower
3 dielectric constant. In this way, prior to the
4 initiation of conduction through the phosphor layer, the
5 voltage across a pixel can be largely across the
6 phosphor layer, provided the dielectric layer has a
7 sufficiently high dielectric constant. The
8 present invention provides an EL laminate, and method of
9 manufacturing same, with a novel and improved dielectric
10 layer. The dielectric layer is formed as a thick layer
11 from a ceramic material to provide:

12 - a dielectric strength greater than about 1.0
13 $\times 10^6$ V/m;

14 - a dielectric constant such that the ratio of
15 the dielectric constant of dielectric material (k_2) to
16 that of the phosphor layer (k_1) is greater than about
17 50:1 (preferably greater than 100:1);

18 - a thickness such that the ratio of the
19 thickness of the dielectric layer (d_2) to that of the
20 phosphor layer (d_1) is in the range of about 20:1 to
21 500:1 (preferably 40:1 to 300:1); and

22 - a surface adjacent the phosphor layer which
23 is compatible with the phosphor layer and sufficiently
24 smooth that the phosphor layer illuminates generally
25 uniformly at a given excitation voltage.

26 The laminate including the dielectric layer of
27 the present invention is most preferably one in which
28 the phosphor layer is a thin film layer. A typical thin
29 film phosphor layer is formed from ZnS:Mn with a
30 thickness of about 0.2 to 2.0 microns, typically about
31 0.5 microns. The material ZnS:Mn has a dielectric
32 constant of about 5 to 10. From theoretical
33 calculations, based on this most preferred phosphor
34 layer (see guidelines set out hereinabove), the
35 dielectric layer of the present invention preferably has
36 a dielectric constant greater than about 500, and most
37 preferably greater than about 1000, and a thickness in

1 the range of about 10 - 300 microns and preferably in
2 the range of 20 - 150 microns. To achieve the high
3 dielectric constant, ferroelectric materials are
4 preferred, most preferably those having a perovskite
5 crystal structure. Exemplary materials include PbNbO₃,
6 BaTiO₃, SrTiO₃, and PbTiO₃.

7 The dielectric layer of this invention is
8 formed in a laminate which is constructed from the rear
9 to the front. The rear electrode is thus deposited on
10 a substrate, most preferably a ceramic such as alumina,
11 which can withstand higher temperatures in manufacture
12 than can glass substrates (used in front to rear TFEL
13 construction in order to provide front transparency).
14 The dielectric layer of the invention is then deposited,
15 by thick film techniques, on the rear electrode. It is
16 then sintered at a high temperature, but one which can
17 be withstood by the substrate and rear electrode. The
18 use of thick film techniques and high temperature
19 sintering is important to the overall properties of the
20 dielectric layer because a dense layer with a high
21 degree of crystallinity is achieved, which improves the
22 overall dielectric constant and dielectric strength of
23 the layer.

24 In practice, the inventors have found that it
25 is difficult to produce the desired surface of the
26 dielectric adjacent the phosphor layer (i.e. compatible
27 and smooth) with the presently available ceramic
28 materials. Thus, in a preferred embodiment of the
29 invention, the dielectric layer is formed as two layers,
30 a first dielectric layer formed on the rear electrode
31 and having the preferred high dielectric strength and
32 dielectric constant values set out hereinabove, and a
33 second dielectric layer which provides the surface
34 adjacent the phosphor layer as set out above.

35 In a preferred embodiment of the invention,
36 the first dielectric layer is deposited by thick film
37 techniques (preferably screen printing) followed by high

1 temperature sintering (preferably less than the melting
2 point of all lower layers, typically less than 1000°C).
3 Pastes containing ferroelectric ceramics, preferably
4 having perovskite crystal structures, as set above are
5 preferred materials, provided the paste formulation
6 permits sintering at the high sintering temperature.
7 The second dielectric layer is preferably deposited by
8 sol gel techniques, followed by high temperature
9 sintering, to provide a smooth surface. The material
10 used in the second layer preferably provides a high
11 dielectric constant (preferably greater than 20, more
12 preferably greater than 100) and a thickness greater
13 than 2 microns (preferably 2 - 10 microns).
14 Ferroelectric ceramics with perovskite crystal
15 structures are most preferred.

16 The invention has been demonstrated with a
17 first dielectric layer screen printed from lead niobate
18 with a thickness of 30 microns, and a second dielectric
19 layer spin deposited as a sol from lead zirconate
20 titanate with a thickness of 2 - 3 microns. The sol gel
21 layer has also been demonstrated by dipping to form
22 several layers with a total thickness of 6-10 microns.
23 Lead lanthanum zirconate titanate is also demonstrated
24 as a sol gel layer.

25 The use of a two layer dielectric, while not
26 essential, has its advantages. While the first
27 dielectric layer is formed as a thick layer with the
28 needed high dielectric strength and high dielectric
29 constant, the second layer is not so limited. Provided
30 the second layer has the desired compatible and smooth
31 surface, it can be formed as a thinner layer from
32 different materials than used in the first layer. Much
33 research has been done on altering the properties of the
34 dielectric - phosphor interface of EL laminates, for
35 instance to improve chemical stability or injectivity.
36 Materials or deposition techniques including these
37 improvements can be used with the first and/or second

1 dielectric layers of this invention, for instance in the
2 choice of materials or deposition techniques used in the
3 first or second layer, by altering the surface of the
4 second layer, or by applying a further thin film layer
5 of a third material above the first or second layer.

6 Laminates made in accordance with the present
7 invention have been demonstrated to exhibit good
8 luminosity without breakdown at low operating voltages.
9 The preferred thick film and sol gel deposition
10 techniques for the dielectric layer(s) are generally
11 simple and inexpensive techniques compared to the thin
12 film techniques described hereinabove. Another
13 advantage of the dielectric layer(s) of this invention
14 is that laminates incorporating the layer(s) do not
15 require a further dielectric layer between the phosphor
16 layer and the second electrode, although such a further
17 dielectric layer may be included if desired.

18 Thus, in one broad aspect, the invention
19 provides a dielectric layer in an electroluminescent
20 laminate of the type including a phosphor layer
21 sandwiched between a front and a rear electrode, the
22 rear electrode being formed on a substrate and the
23 phosphor layer being separated from the rear electrode
24 by a dielectric layer. The dielectric layer comprises
25 a planar layer formed from a ceramic material providing
26 a dielectric strength greater than about 1.0×10^6 V/m
27 and a dielectric constant such that the ratio of k_2/k_1 is
28 greater than about 50:1, the dielectric layer having a
29 thickness such that the ratio of $d_2:d_1$ is in the range of
30 about 20:1 to 500:1, and the dielectric layer having a
31 surface adjacent the phosphor layer which is compatible
32 with the phosphor layer and sufficiently smooth that the
33 phosphor layer illuminates generally uniformly at a
34 given excitation voltage.

35 The invention also broadly extends to a method
36 of forming a dielectric layer in an electroluminescent
37 laminate of the type including a phosphor layer

1 sandwiched between a front and a rear electrode, the
2 rear electrode being formed on a substrate and the
3 phosphor layer being separated from the rear electrode
4 by a dielectric layer. The method comprises depositing
5 on the rear electrode, by thick film techniques followed
6 by sintering, a ceramic material having a dielectric
7 constant such that the ratio of k_2/k_1 is greater than
8 about 50:1, to form a dielectric layer having a
9 dielectric strength greater than about 1.0×10^6 V/m and
10 a thickness such that the ratio of d_2/d_1 is in the range
11 of about 20:1 to 500:1, the dielectric layer forming a
12 surface adjacent the phosphor layer which is compatible
13 with the phosphor layer and sufficiently smooth that the
14 phosphor layer illuminates generally uniformly at a
15 given excitation voltage.

16 This invention also broadly provides a process
17 for laser scribing a pattern in a planar laminate having
18 at least one overlying layer and at least one underlying
19 layer, comprising:

20 applying a focused laser beam on the overlying
21 layer side of the laminate, said laser beam having a
22 wavelength which is substantially unabsorbed by the
23 overlying layer but which is absorbed by the underlying
24 layer, such that at least a portion of the underlying
25 layer is directly ablated and the overlying layer is
26 indirectly ablated throughout its thickness.

27 In the context of an EL laminate, the
28 overlying layers are the transparent conductive material
29 and the phosphor, the underlying layers are one or more
30 dielectric layers and the pattern is an electrode
31 pattern of parallel spaced address lines.

32 Throughout the specification and the claims,
33 the following definitions apply:

34 Absorption occurs in a material when a quantum
35 of radiant energy coincides with an allowed transition
36 within the material to a higher energy state, for

1 example by promotion of electrons across the band gap
2 for that material.

3 Direct ablation of a material by a laser beam
4 occurs when the dominant cause of ablation is
5 decomposition and/or due to absorption of the radiant
6 energy of the laser beam by the material.

7 Indirect ablation of a material by a laser
8 beam occurs when the dominant cause of ablation is
9 vaporization due to heat generated in, and transported
10 from, an adjacent material which absorbs the radiant
11 energy of the laser beam.

12 The invention also extends to an
13 electroluminescent display panel providing for
14 electrical connection from a planar electroluminescent
15 laminate to the output of one or more voltage driving
16 components of a driver circuit using through hole
17 connectors. The display panel includes:

18 - an electroluminescent laminate formed on a
19 rear substrate and having front and rear sets of
20 intersecting address lines such as is known in the art;

21 - a plurality of through holes formed in the
22 substrate adjacent the ends of the address lines; and

23 - means forming a conductive path through each
24 of the through holes in the substrate to the ends of
25 each of the address lines to provide for electrical
26 connection of each address line to a voltage driving
27 component of the driving circuit.

28 Preferably, the electroluminescent laminate of
29 the display panel includes the thick film dielectric
30 layer of the present invention. This dielectric layer
31 enables the laminate to be constructed from the rear
32 substrate toward the front viewing side, which in turn
33 enables the through hole connectors and thick film
34 circuit patterns for connection to the voltage driving
35 components and address lines to be formed by
36 interleaving the circuit fabrication steps with the
37 fabrication steps for the electroluminescent laminate.

Such steps could not easily be accomplished in the construction of a conventional electroluminescent laminate since the layers are deposited on the front display glass which will not withstand temperatures to fire thick film conductive pastes.

In accordance with the present invention, the voltage driving components or the entire driving circuit may be formed on the rear (reverse) side of the rear substrate. The use of through hole connectors provides for more direct, highly reliable interconnections between the address lines and the driving circuit. A non-active perimeter around the display panel, as is needed in the prior art, is not needed. This facilitates the assembly of large displays from individual display panels without dark boundaries between the modules.

DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic, cross sectional view of the laminate structure including a two layer dielectric of the present invention; and

Figure 2 is a top view of the laminate structure of Figure 1.

Figure 3 is a schematic cross sectional view of the laminate structure along a column electrode showing the preferred embodiment of connecting the row and column electrode address lines to the voltage driving components of the voltage driving circuit;

Figure 4 is a top view of the rear substrate with the preferred pattern of through holes for electrical connection of the address lines to the voltage driving components of the driver circuit;

Figure 5 is a top view of a preferred driver circuit pattern printed on the rear side of the rear substrate;

1 Figure 6 is a top view of the row electrodes
2 and column pads printed on the front side of the rear
3 substrate;

4 Figure 7 is a top view of the circuit pad
5 reinforcement pattern preferably printed over the driver
6 circuit pattern of Figure 5;

7 Figure 8 is a top view of the sealing glass
8 pattern preferably printed over the driver circuit
9 pattern and circuit pad reinforcement pattern of Figures
10 5 and 7;

11 Figure 9 is a top view of the column electrode
12 line pattern; and

13 Figure 10 is a top view of the electrical
14 connections printed between the column lines of Figure
15 9 and the column pads of Figure 6.

16 DESCRIPTION OF THE PREFERRED EMBODIMENTS

17 An EL laminate 10 incorporating a two layer
18 dielectric in accordance with the present invention is
19 illustrated in Figures 1 and 2. The laminate 10 is
20 built from the rear side on a substrate 12. A rear
21 electrode layer 14 is formed on the substrate 12. As
22 shown in the Figures, for display applications, the rear
23 electrode 14 consists of rows of conductive address
24 lines centered on the substrate 12 and spaced from the
25 substrate edges. An electric contact tab 16 protrudes
26 from the electrode 14. A first, thick dielectric layer
27 18 is formed above the rear electrode 14, followed by a
28 second, thinner dielectric layer 20. A phosphor layer
29 22 is formed above the second dielectric layer 20,
30 followed by a front, transparent electrode layer 24.
31 The front electrode layer 24 is shown in the Figures as
32 solid, but in actuality, for display applications, it
33 consists of columns of address lines arranged
34 perpendicular to the address lines of the rear electrode
35 14. The laminate 10 is encapsulated with a transparent
36 sealing layer 26 to prevent moisture penetration. An

1 electric contact 28 is provided to the second electrode
2 24.

3 The EL laminate 10 is operated by connecting
4 an AC power source to the electrode contacts 16, 28. An
5 EL laminate in accordance with the invention has utility
6 as lamps or displays, although it will most frequently
7 find application in displays.

8 It will be understood by persons skilled in
9 the art that further intervening layers can be included
10 in the laminate 10 without departing from the present
11 invention.

12 A method of constructing a double dielectric
13 layer in an EL laminate, in accordance with the
14 invention, will now be described with preferred
15 materials and process steps.

16 The laminate 10 is constructed from the rear
17 to the front (viewing) side. The laminate 10 is formed
18 on a suitable substrate 12. The substrate 12 is
19 preferably a ceramic which can withstand the high
20 sintering temperatures (typically 1000°C) used in the
21 dielectric layer. Alumina is most preferred.

22 Deposited on the substrate 12 is the first,
23 rear electrode 14. Many techniques and materials are
24 known for laying down thin rows of address lines.
25 Preferably, conductive metal address lines are screen
26 printed from a Ag/Pt alloy paste, using an emulsion
27 which can be washed away in the areas where the paste is
28 to be printed. The paste is thereafter dried and fired.
29 Alternatively, the rear electrode 14 may be formed from
30 other noble metals such as gold, or other metals such as
31 chromium, tungsten, molybdenum, tantalum or alloys of
32 these metals.

33 The first dielectric layer 18 is deposited on
34 the rear electrode by known thick film techniques. The
35 first dielectric layer 18 is preferably formed from a
36 ferroelectric material, most preferably one having a high
37 perovskite crystal structure, to provide a high

1 dielectric constant compared to that of the phosphor
2 layer 22. The material will have a minimum dielectric
3 constant of 500 over a reasonable operating temperature
4 for the laminate, generally 20 - 100°C. More preferably,
5 the dielectric constant of the first dielectric layer
6 material is 1000 or greater. Exemplary materials for
7 the first dielectric layer 18 include $PbNbO_3$, $BaTiO_3$,
8 $SrTiO_3$, and $PbTiO_3$, $PbNbO$, being particularly preferred.

9 As will be understood by persons skilled in
10 this art, in choosing a ceramic material (i.e. an
11 electrical insulating material having a melting point
12 which is sufficiently high to allow for the preparation
13 of the other layers of the laminate) for the first
14 dielectric layer 18, one chooses materials known to have
15 high dielectric constants and dielectric strengths.
16 These are intrinsic properties of the materials,
17 however, the values are generally given for bulk
18 materials, which are present in a dense, highly
19 crystalline form. The deposition techniques used can
20 alter these properties. In respect of the dielectric
21 constant of the material, the thick film deposition
22 techniques, followed by high temperature sintering, will
23 generally preserve a large particle size (in the range
24 of about 1 micron to about 2 microns) and a high degree
25 of crystallinity in a dense structure, so as not to
26 significantly lower the dielectric constant from that of
27 the starting material. Similarly, a high dielectric
28 strength is achieved using thick film deposition
29 techniques followed by high temperature sintering.
30 However, the dielectric strength of the layer(s) should
31 ultimately be measured by imposing an operating voltage
32 across the completed laminate.

33 Thick film deposition techniques are known in
34 the art, as set forth above. By such techniques, the
35 dielectric material is deposited on the rear electrode
36 layer 14 to the desired thickness with generally uniform
37 coverage. Thick film deposition techniques are

1 frequently used in the manufacture of electronic
2 circuits on ceramic substrates. Screen printing is the
3 most preferred technique. Commercially available
4 dielectric pastes can be used, with the recommended
5 sintering steps set out by the paste manufacturers.
6 Pastes should be chosen or formulated to permit
7 sintering at a high temperature, typically about 1000°C.
8 However, other techniques can achieve similar results.
9 One alternate thick film technique is the use a
10 dielectric as a "green tape", such that it can be laid
11 down on the rear electrode 14. The green tape comprises
12 a dielectric powder in a polymeric matrix that can be
13 burned out during the subsequent sintering process. The
14 tape is flexible before sintering, and can be rolled or
15 pressed onto the electrode layer 14. One possible
16 advantage of the green tape over the screen printed
17 dielectric is that it may be somewhat more dense with
18 fewer pores once it is fired. At present, green tape
19 dielectrics are not widely available. Thick film pastes
20 of the dielectric can also be roll coated onto the rear
21 electrode layer 14, or applied with a doctor blade.
22 More complex techniques such as electrostatic deposition
23 of a dielectric powder followed by immediate sintering
24 before the powder loses its electrostatic charge may
25 also be used.

26 As indicated, the first dielectric layer 18 is
27 preferably screen printed from a paste. Depositing in
28 multiple layers followed by sintering at a high
29 temperature is preferred in order to achieve low
30 porosity, high crystallinity and minimal cracking. The
31 sintering temperature will depend on the particular
32 material being used, but will not exceed the temperature
33 which the rear electrode 14 or substrate 12 can
34 withstand. A temperature of 1000°C is typically the
35 maximum for most electrode materials. The thickness of
36 the first dielectric layer 18 will vary with its
37 dielectric constant and with the dielectric constants

1 and thicknesses of the phosphor layer 22 and the second
2 dielectric layer 20. Generally, the thickness of the
3 first dielectric layer 18 is in the range of 10 to 300
4 microns, preferably 20 - 150 microns, and more
5 preferably 30 - 100 microns.

6 It will be appreciated that, in general, the
7 criteria for establishing the thickness and dielectric
8 constant of the dielectric layer(s) are calculated so as
9 to provide adequate dielectric strength at minimal
10 operating voltages. The criteria are interrelated, as
11 set forth below. Given a typical range of thickness for
12 the phosphor layer (d_1) of between about 0.2 and 2.0
13 microns, a dielectric constant range for the phosphor
14 layer (k_1) of between about 5 and 10 and a dielectric
15 strength range for the dielectric layer(s) of about 10^6
16 to 10^7 V/m, the following relationships and calculations
17 can be used to determine typical thickness (d_2) and
18 dielectric constant (k_2) values for the dielectric layer
19 of the present invention. These relationships and
20 calculations may be used as guidelines to determine d_2
21 and k_2 values, without departing from the intended scope
22 of the present invention, should the typical ranges set
23 out hereinabove change significantly.

24 The applied voltage V across a bilayer
25 comprising a uniform dielectric layer and a uniform non-
26 conducting phosphor layer sandwiched between two
27 conductive electrodes is given by equation 1:

$$V = E_2 * d_2 + E_1 * d_1 \quad (1)$$

29 wherein:

30 E_2 is the electric field strength in the
31 dielectric layer;

32 E_1 is the electric field strength in the
33 phosphor layer;

34 d_2 is the thickness of the dielectric layer;
35 and

36 d_1 is the thickness of the phosphor.

1 In these calculations, the electric field
2 direction is perpendicular to the interface between the
3 phosphor layer and the dielectric layer. Equation 1
4 holds true for applied voltages below the threshold
5 voltage at which the electric field strength in the
6 phosphor layer is sufficiently high that the phosphor
7 begins to break down electrically and the device begins
8 to emit light.

9 From electromagnetic theory, the component of
10 electric displacement D perpendicular to an interface
11 between two insulating materials with different
12 dielectric constants is continuous across the interface.
13 This electric displacement component in a material is
14 defined as the product of the dielectric constant and
15 the electric field component in the same direction.
16 From this relationship equation 2 is derived for the
17 interface in the bilayer structure:

18 $k_2 * E_2 = k_1 * E_1 \quad (2)$

19 wherein:

20 k_2 is the dielectric constant of the dielectric
21 material; and

22 k_1 is the dielectric constant of the phosphor
23 material.

24 Equations 1 and 2 can be combined to give
25 equation 3:

26 $V = (k_1 * d_2 / k_2 + d_1) * E_1 \quad (3)$

27 To minimize the threshold voltage, the first
28 term in equation 3 needs to be as small as is practical.
29 The second term is fixed by the requirement to choose
30 the phosphor thickness to maximize the phosphor light
31 output. For this evaluation the first term is taken to
32 be one tenth the magnitude of the second term.
33 Substituting this condition into equation 3 yields
34 equation 4:

35 $d_2 / k_2 = 0.1 * d_1 / k_1 \quad (4)$

36 Equation 4 establishes the ratio of the
37 thickness of the dielectric layer to its dielectric

1 constant in terms of the phosphor properties. This
2 thickness is determined independently from the
3 requirement that the dielectric strength of the layer be
4 sufficient to hold the entire applied voltage when the
5 phosphor layer becomes conductive above the threshold
6 voltage. The thickness is calculated using equation 5:
7

$$d_2 = V/S \quad (5)$$

8 wherein:

9 S is the strength of the dielectric material.

10 Use of the above equations and reasonable
11 values for d_1 , k_1 , and S provides the range of dielectric
12 layer thickness and dielectric constant set forth in
13 this specification and claims.

14 As stated previously, a second dielectric
15 layer 20 is not needed if the first dielectric layer 22
16 provides a surface adjacent the phosphor layer which is
17 sufficiently smooth (i.e. a subsequently deposited
18 phosphor layer will illuminate generally uniformly at a
19 given excitation voltage) and is compatible with the
20 phosphor layer 22. Generally, a surface relief that
21 does not vary more than about 0.5 microns over about
22 1000 microns (which equates approximately to a pixel
23 width) is sufficient. A surface relief of 0.1 - 0.2
24 microns over that distance is more preferred. If the
25 first dielectric layer 18 provides a sufficiently smooth
26 surface, but does not provide the desired compatibility
27 with the phosphor layer 22, a further layer of material
28 (preferably, but not necessarily a dielectric material)
29 to provide that compatibility may be added, for instance
30 by thin film techniques.

31 In the event that the second dielectric layer
32 20 is needed, it is formed on the first dielectric layer
33 18. The second layer 20 may have a lower dielectric
34 constant than that of the first dielectric layer 18 and
35 will typically be formed as a much thinner layer
36 (preferably greater than 2 microns and more preferably
37 2 - 10 microns). The desired thickness of second

1 dielectric layer is generally a function of smoothness,
2 that is the layer may be as thin as possible, provided
3 a smooth surface is achieved. To provide a smooth
4 surface, sol gel deposition techniques are preferably
5 used, followed by high temperature sintering. Sol gel
6 deposition techniques are well understood in the art,
7 see for example "Fundamental Principles of Sol Gel
8 Technology", R.W. Jones, The Institute of Metals, 1989.
9 In general, the sol gel process enables materials to be
10 mixed on a molecular level in the sol before being
11 brought out of solution either as a colloidal gel or a
12 polymerizing macromolecular network, while still
13 retaining the solvent. The solvent, when removed,
14 leaves a solid with a high level of fine porosity,
15 therefore raising the value of the surface free energy,
16 enabling the solid to be sintered and densified at lower
17 temperatures than obtainable using most other
18 techniques.

19 The sol gel materials are deposited on the
20 first dielectric layer 18 in a manner to achieve a
21 smooth surface. In addition to providing a smooth
22 surface, the sol gel process facilitates filling of
23 pores in the sintered thick film layer. Spin deposition
24 or dipping are most preferred. These are techniques
25 used in the semiconductor industry for many years,
26 mainly in photolithography processes. For spin
27 deposition, the sol material is dropped onto the first
28 dielectric layer 18 which is spinning at a high speed,
29 typically a few thousand RPM. The sol can be deposited
30 in several stages if desired. The thickness of the
31 layer 20 is controlled by varying the viscosity of the
32 sol gel and by altering the spinning speed. After
33 spinning, a thin layer of wet sol gel is formed on the
34 surface. The sol gel layer 20 is sintered, generally at
35 less than 1000°C, to form a ceramic surface. The sol may
36 also be deposited by dipping. The surface to be coated
37 is dipped into the sol and then pulled out at a constant

1 speed, usually very slowly. The thickness of the layer
2 is controlled by altering the viscosity of the sol and
3 the pulling speed. The sol may also be screen printed
4 or spray coated, although it is more difficult to
5 control the thickness of the layer with these
6 techniques.

7 The material used in the second dielectric
8 layer 20 is preferably a ferroelectric ceramic material,
9 preferably having a perovskite crystal structure to
10 provide a high dielectric constant. The dielectric
11 constant is preferably similar to that of the first
12 dielectric layer material in order to avoid voltage
13 fluctuations across the two dielectric layers 18, 20.
14 However, with a thinner layer being utilized in the
15 second dielectric 20, a dielectric constant as low as
16 about 20 may be used, but will preferably be greater
17 than 100. Exemplary materials include lead zirconate
18 titanate (PZT), lead lanthanum zirconate titanate
19 (PLZT), and the titanates of Sr, Pb and Ba used in the
20 first dielectric layer 18, PZT and PLZT being most
21 preferred.

22 PZT or PLZT are preferably deposited as a sol
23 gel by spin deposition followed by sintering at less
24 than about 600°C, to form a smooth ceramic surface
25 suitable for deposition of the next layer.

26 The next layer to be deposited will typically
27 be the phosphor layer 22, however, as set out
28 hereinabove, it is possible, within the scope of this
29 invention to include a further layer above the second
30 dielectric layer 20 to further improve the interface
31 with the phosphor layer. For instance, a thin film
32 layer of material known to provide good injectivity and
33 compatibility may be used.

34 The phosphor layer 22 is deposited by known
35 thin film deposition techniques such as vacuum
36 evaporation with an electron beam evaporator, sputtering
37 etc. The preferred phosphor material is ZnS:Mn, but

1 other phosphors that emit light of different colours are
2 known. The phosphor layer 22 typically has a thickness
3 of about 0.5 microns and a dielectric constant between
4 about 5 and 10.

5 A further transparent dielectric layer above
6 the phosphor layer 22 is not needed, but may be included
7 if desired.

8 The front electrode layer 24 is deposited
9 directly on the phosphor layer 22 (or the further
10 dielectric layer if included). The front electrode is
11 transparent and is preferably formed from indium tin
12 oxide (ITO) by known thin film deposition techniques
13 such as vacuum evaporation in an electron beam
14 evaporator.

15 The laminate 10 is typically annealed and then
16 sealed with a sealing layer 26, such as glass.

17 A preferred laminate, from rear to front, with
18 typical thickness values in accordance with the present
19 invention is as follows:

20 Substrate Layer - Alumina
21 Rear Electrode - Ag/Pt Address lines - 10 microns
22 First Dielectric Layer - Lead Niobate - 30 microns
23 Second Dielectric Layer - Lead Zirconate Titanate - 2
24 microns
25 Phosphor Layer - ZnS:Mn - 0.5 microns
26 Front Electrode - ITO - 0.1 microns
27 Sealing Layer - Glass - 10 - 20 microns.

28 In larger EL displays, the thicknesses of the
29 layers may vary. For instance, the sol gel layer
30 thickness is typically increased to about 6-10 microns
31 to provide the desired smoothness. Similarly, the ITO
32 layer thickness might be increased up to 0.3 microns in
33 a larger display.

34 In accordance with the present invention the
35 connection of the front and rear address lines of an
36 electroluminescent laminate to the voltage driver
37 circuit is preferably achieved using the through hole in
38 the rear substrate. Most preferably, the EL laminate

1 includes the thick dielectric layer of this invention,
2 although this is not necessary.

3 Voltage driver circuitry includes voltage
4 driving components (typically referred to as high
5 voltage driver chips), the outputs of which are
6 connected to the individual row and column address lines
7 of the rear and front electrodes in order to selectively
8 activate pixels in accordance with the video input
9 signals. The voltage driver circuitry and components
10 are generally known in the art. To illustrate the
11 present invention, through hole connections were
12 provided for known packaged high voltage driver chips
13 which are to be surface mounted on the rear substrate by
14 known reflow soldering techniques. Such high voltage
15 driver chips are known for the conventional symmetric
16 pulse driving schemes and for asymmetric pulse driving
17 schemes.

18 However, it will be realized by those skilled
19 in the art that the particular driver circuitry or
20 driver components may be varied and as such will
21 naturally affect the patterns of through holes and the
22 circuit patterns provided for connection to the driver
23 circuitry. The invention has application whether the
24 entire driving circuit or only a portion thereof is to
25 be mounted on the rear substrate. For instance, instead
26 of using the high voltage packaged chips, it is possible
27 to use bare silicon die (chips) on the substrate using
28 conventional die attach methods, and using conventional
29 wirebonding techniques to connect the chips to the drive
30 circuitry on the substrate. In this case, the driver
31 chips would occupy much less area on the substrate and
32 it would be possible to place all of the drive circuitry
33 on the substrate. The result is an ultrathin display
34 panel that could be interfaced directly to a video
35 signal and connected directly to a dc power supply.
36 Such displays would be useful in ultrathin portable
37 products that require a display. Of course, the ability

1 to mount driving circuitry on the rear of the substrate
2 is tied to the overall size of the display, a larger
3 display providing more space for the drive circuitry
4 directly on the rear of the substrate.

5 The circuit connection aspect of this
6 invention is illustrated in Figures 3 - 10. As
7 indicated above, particular through hole and circuit
8 patterns are provided for illustration purposes for
9 mounting high voltage driver chips 30 on the reverse
10 side of the rear substrate. The particular chips chosen
11 were Supertex HV7022PJ chips to connect to the row
12 address lines 14 and Supertex HV8308PJ and HV8408PJ
13 (Supertex Inc. is located in Sunnyvale, California) for
14 connection to the column address lines 24. The latter
15 two chips differ in that the lead pattern of one is a
16 mirror image of the lead pattern of the other.

17 Referring to the Figures, the EL laminate 10
18 is preferably, but not necessarily, constructed with the
19 two layer dielectric layers 18, 20 of this invention,
20 and is thus constructed from the rear substrate 12
21 toward the front viewing side. The rear substrate 12 is
22 drilled with through holes 32 in a pattern such that
23 they will be proximate the ends of the address lines 14,
24 24 (subsequently formed). Alternatively, additional
25 through holes could be provided in a spaced relationship
26 along the address lines. This would be useful to
27 provide connection to front ITO address lines which have
28 high resistivity. The pattern of Figure 4 provides for
29 connection to an EL laminate 10 on a rectangular
30 substrate 12, with row address lines (rear electrode) 14
31 along the longer dimension and column address lines
32 (front electrode) 24 along the shorter dimension.

33 The through holes 32 are preferably formed by
34 laser. The holes 32 are typically wider on one side due
35 to the nature of the laser drilling process, that side
36 being chosen to be the rear or reverse side to
37 facilitate flowing conductive material into the holes.

1 The substrate 12 used in the EL laminate
2 should be one which can withstand the temperatures
3 encountered in the subsequent processing steps.
4 Typically substrates used are those which provide
5 sufficient rigidity to support the laminate and which
6 are stable to temperatures of 850°C or greater to
7 withstand the subsequent firing sintering steps for the
8 thick film pastes and sol gel materials. The substrate
9 should also be opaque to laser light, to allow the
10 through holes 32 to be formed by laser drilling.
11 Finally, the substrate should provide for good adherence
12 of the thick film pastes used in subsequent steps.
13 Crystalline ceramic materials and opaque vitreous
14 materials may be used. Alumina is particularly
15 preferred.

16 A circuit pattern 34 of conductive material is
17 printed on the rear side of the substrate 12 in the
18 pattern shown in Figure 5. In this step, the conductive
19 material is pulled through the through holes 32 in a
20 manner to be discussed. The circuit pattern 34 on the
21 rear side of the substrate 12 consists of rear connector
22 pads 36 around each of the through holes 32, chip
23 connector pads 38 for the outputs of the high voltage
24 driver chips (not shown), further connector pads (not
25 labelled) for connection to the rest of the drive
26 circuit (not shown), and electrical leads (not labelled)
27 between numerous of the connector pads as shown.

28 The conductive material is preferably a
29 conductive thick film paste applied by screen printing.
30 Silver/platinum thick film pastes are preferred.

31 To form a conductive path through each through
32 hole 32, a vacuum is applied on the front side of the
33 substrate 12 while the circuit 34 is printed on the rear
34 side. This is preferably accomplished by placing the
35 substrate 12 on a vacuum table with a master plate
36 having holes drilled in the pattern of Figure 4 between
37 the substrate 12 and the vacuum. The holes in the master

1 plate are aligned with and somewhat larger than the
2 holes in the substrate 12. The vacuum is not applied
3 until the circuit is printed to ensure that the vacuum
4 is uniformly applied. The vacuum is continued until
5 conductive material is pulled through to the front side
6 of the substrate. At that point, a small amount of the
7 conductive material is pulled through to the front side
8 of the substrate 12 and the through hole walls are
9 coated. The thick film paste is then fired in
10 accordance with known procedures.

11 Following this step a circuit pad
12 reinforcement pattern 42 is preferably, but not
13 necessarily, printed as shown in Figure 7. Similar
14 conductive materials, printing and firing steps are
15 followed.

16 The row address lines 14 and connector pads
17 40a and 40b are then formed on the front side of the
18 substrate 12, preferably by screen printing a thick film
19 conductive paste such as a silver/platinum paste. The
20 address line pattern is shown in Figure 6 to include
21 rows extending along the length of the substrate 12 and
22 ending at the front (row) connector pads 40a. During
23 this same step, the front (column) connector pads 40b
24 are printed to provide for ultimate connection of the
25 column address lines to the driving circuitry via the
26 through holes 32. The conductive paste is preferably
27 pulled through the through holes 32 as above, with the
28 vacuum being applied from the rear, circuit side of the
29 substrate.

30 While the means forming a conductive path
31 through the through holes 32 has been set out above to
32 be formed from thick film conductive pastes, the
33 conductive paths might also be formed as electroplated
34 through holes, or as through holes formed by electroless
35 plating, as is known in the art, provided the
36 electroplated material adheres properly to the substrate

1 and that subsequent layers adhere to the plated
2 conductor.

3 The thick film dielectric layer 18 of this
4 invention is then preferably formed and fired in the
5 manner set out above.

6 The rear circuit side of the substrate is then
7 preferably sealed, with a rear sealant 44, for instance
8 by screen printing with a thick film glass paste,
9 leaving the connector pads exposed for attachment of the
10 high voltage driver chips and connector pins 45 to the
11 rest of the driver circuitry (not shown). The sealing
12 pattern is shown in Figure 8.

13 The EL laminate is then completed with the sol
14 gel layer 20, the phosphor layer 22 and the front column
15 address lines 24, as described above. The pattern for
16 the front column address lines 24 is shown in Figure 9
17 to consist of parallel columns across the width of the
18 substrate 12 ending proximate the front (column)
19 connector pads 40.

20 Electrical interconnects 46 between the column
21 address lines 24 and the front (column) connector pads
22 40 are provided, if necessary, for reliable electrical
23 connection. These are preferably formed by printing a
24 conductive material such as silver through a shadow mask
25 in the pattern shown in Figure 10.

26 A front sealing layer 26 as previously
27 described is provided to prevent moisture penetration.

28 In accordance with the present invention, the
29 front ITO address lines 24 of the EL laminate 10 are
30 preferably formed by laser scribing. This laser
31 scribing technique is set forth hereinbelow in
32 connection with the preferred EL laminate 10 of this
33 invention. However, it should be understood that the
34 laser scribing technique has broader application in
35 patterning a planar laminate having overlying and
36 underlying layers. In that respect, the ITO and
37 phosphor layers 24, 22 are illustrative of overlying

1 layers which do not absorb the laser light to any
2 substantial extent, and the thick film lead niobate
3 dielectric layer 18 and the sol gel layer 20 of lead
4 zirconate titanate are illustrative of underlying layers
5 that do absorb the laser light. Other typical materials
6 used as transparent conductors include SnO_2 and In_2O_3 .

7 Generally, in the broad context of the
8 invention, the overlying layer is a material which is
9 transparent to visible light and the underlying layer is
10 a material which is opaque to visible light. The
11 underlying material can then be directly ablated, and
12 the overlying material indirectly ablated, by utilizing
13 a laser beam with a wavelength in the visible or
14 infrared region of the electromagnetic spectrum. This
15 laser ablation method has broad application in
16 patterning transparent conductive layers in
17 semiconductors, liquid crystal displays, solar cells,
18 and EL displays.

19 In order to control the precision and
20 resolution of the laser scribing (depth and width of
21 cuts), to avoid explosive delamination of the layers and
22 to minimize interdiffusion between the layers, certain
23 properties of the materials and thicknesses of the
24 layers should be observed.

25 In respect of a two layer laminate, the
26 following relationship should hold:

$$\alpha_u T_u > \alpha_o T_o,$$

28 wherein:

29 α_u = absorption coefficient of underlying layer;

30 α_o = absorption coefficient of overlying layer;

31 T_u = thickness of underlying layer; and

32 T_o = thickness of overlying layer.

33 More preferably, the product of $\alpha_u T_u$ is very
34 much greater than the product of $\alpha_o T_o$.

35 When there is a plurality of overlying
36 transparent layers and/or a plurality of underlying
37 opaque layers, the sum of the product of $\alpha_u T_u$ for each

1 layer should be greater than the sum of the product of
2 $\alpha_o T_o$, for each layer, i.e.

3
$$\sum_i \alpha_{u_i} T_{u_i} > \sum_i \alpha_o T_o ;$$

4 If the above relationship is maintained, it
5 should be possible to directly ablate only a portion of
6 the underlying layer, without cutting through its entire
7 thickness, and indirectly ablate through the entire
8 thickness of the overlying layer, in accordance with the
9 process of the invention.

10 Explosive delamination can result if heat or
11 vapour pressure builds up in the underlying layer before
12 the overlying layer can soften and/or vaporize by
13 indirect ablation. Thus, the material in the overlying
14 layer should melt and vaporize at a lower temperature
15 than does the material in the underlying layer.

16 To enhance the ability to make high resolution
17 cuts, the thermal conductivity of the material in the
18 underlying layer is preferably less than that of the
19 material in the overlying layer. The thermal
20 conductivities of both layers should be such that
21 significant heat does not flow away from the region
22 being ablated in the time during which that region is
23 exposed to the laser beam.

24 To avoid mass interdiffusion between layers,
25 the diffusion time for such processes should be greater
26 than the time during which the region to be ablated is
27 exposed to the laser beam.

28 The above preferred properties are generally
29 known for materials, making it possible to predict which
30 materials are amenable to the laser scribing process of
31 this invention.

32 Resolution of the laser cuts, explosive
33 delamination and interdiffusion are also affected by the
34 wavelength, power and scanning speed of the laser beam.
35 However if the above relationships and properties are
36 generally maintained, these other laser conditions can
37 be controlled and varied to achieve the desired results
38 of direct and indirect ablation.

1 Lasers are known which provide a laser beam
2 with a wavelength in the visible or infrared region.
3 Carbon dioxide lasers, argon lasers and YAG lasers are
4 exemplary. All have wavelengths greater than about 400
5 nm. Pulsed or continuous wave (CW) lasers may be used,
6 the latter being preferred to provide sharp, high
7 resolution cuts. The laser beam is focused by
8 appropriate known lens systems to achieve the desired
9 resolution and to ensure sufficient local power density
10 for complete removal of overlying layer. Generally, the
11 power density of the laser beam is set so that the
12 groove which is cut is significantly greater than the
13 thickness of the overlying transparent layers. When the
14 transparent layer comprises electrode address lines,
15 this ensures that the address lines are clearly defined
16 and electrically isolated.

17 Scribing can be performed either by moving the
18 laser beam with respect to the material being scribed or
19 more preferably, by mounting the material to be scribed
20 on an X-Y coordinates table that is moveable relative to
21 the laser beam. For scribing address lines, a table
22 moveable in the X direction (i.e. perpendicular to the
23 lines being scribed) is preferred, the laser beam being
24 moveable in the Y direction, i.e. along the lines.

25 Material which is vaporized or decomposed
26 during the laser scribing process may be drawn away from
27 the material being scribed by a vacuum located proximate
28 to the laser beam.

29 In the preferred EL laminate 10 of the present
30 invention, a thin layer of indium tin oxide 24 is
31 deposited by known methods above the phosphor layer 22.
32 Vacuum deposition methods or sol gel methods to deposit
33 ITO are disclosed in U.S. Patents. 4,568,578 and
34 4,849,252. Materials other than ITO may be used, for
35 example fluorine doped tin oxide. An optional
36 transparent dielectric layer can be provided between the
37 ITO and phosphor layers 24, 22. The preferred sol gel
38 layer 20 of PZT and the thick film dielectric layer 18
39 of lead niobate underlie the phosphor layer. The EL

1 laminate 10 is formed in reverse sequence to
2 conventional TFEL devices, as described hereinabove.
3 This conveniently leaves the ITO layer 24 and the
4 phosphor layer 22 as upper (overlying) transparent
5 layers above lower (underlying) opaque dielectric layers
6 18, 20 (lead niobate and PZT), amenable to laser
7 scribing in accordance with the present invention.

8 The individual column address lines 24 are
9 laser scribed, as described above. The laser beam
10 directly ablates at least a portion of the sol gel layer
11 20 and possibly a minor portion of the thick underlying
12 dielectric layer 18 and indirectly ablates the ITO and
13 phosphor layers 24, 22 throughout their thicknesses.
14 This leaves a reliable insulating gap between the
15 adjacent address lines.

16 The column address lines 24 are connected to
17 the driving circuitry as described above. More
18 particularly, in accordance with the preferred through
19 hole connecting process described above, the electrical
20 interconnects 46 are formed (prior to laser scribing) by
21 evaporating silver in the pattern shown in Figure 10 in
22 locations to overlap the portions of the ITO layer which
23 will ultimately form the address lines. The address
24 lines are then scribed in the manner set out above.

25 The completed EL laminate 10 can be sealed as
26 described above by spraying a protective polymer sealant
27 on the front viewing surface or by bonding a glass plate
28 26 to the front surface.

29 Several advantages are derived by using
30 indirect ablation to scribe transparent conductor
31 materials. A relatively low power continuous wave laser
32 producing light in the visible range can be used rather
33 than an ultraviolet pulsed laser with a high
34 instantaneous power output. This not only reduces laser
35 costs, but produces smoother edges on the ablated cuts.
36 This is particularly important for high resolution EL
37 displays. Direct ablation of transparent materials
38 requires very high instantaneous laser power to deposit
39 the energy necessary for the ablation in a time short

1 enough to prevent diffusion of heat away from the area
2 where ablation is to occur. In prior art attempts to
3 directly ablate a transparent conductor deposited on a
4 transparent substrate, only a small fraction of the
5 laser power is directly absorbed by the transparent
6 conductor material; most of the light passes through
7 both transparent layers. In many cases, indirect
8 ablation can minimize the problem of interdiffusion
9 between layers, since the heating to vaporize the
10 transparent layers occurs from the bottom of the
11 transparent layers. This promotes the removal of
12 ablated material outwardly and upwardly in the stream of
13 vaporized material, rather than diffusion of the
14 material into the underlying layer. This ... is
15 particularly important in order to preserve the quality
16 of the dielectric and phosphor layers in EL displays.

17 The present invention is further illustrated
18 by the following non-limiting examples.

19 EXAMPLE 1

20 This example is included to illustrate that
21 simply screen printing a thick film layer of barium
22 titanate (the material used as a ceramic sheet in the
23 Miyata et al. references) is subject to electric
24 breakdown under operating conditions of about 200V.

25 A single pixel electroluminescent device was
26 constructed on an alumina substrate (5 cm square, 0.1 cm
27 thick) obtained from Coors Ceramics (Grand Junction,
28 Colorado, U.S.A.). A rear electrode layer was applied,
29 centered on the substrate, but spaced from the edges.
30 The material used was a silver/platinum conductor which
31 was printed as address lines as is conventional in
32 electronics. More particularly, Cermalloy # C4740
33 (available from Cermalloy, Conshohocken, Pa.) was screen
34 printed as a thick film paste through a 320 mesh
35 stainless steel screen and coated with an emulsion. The
36 emulsion was exposed to ultraviolet light through a
37 photomask, so as to expose those areas of the emulsion
38 that were to be retained for printing. The unexposed
39 emulsion was dissolved away with water where paste was

1 to be printed through the screen. The remaining
2 emulsion was then further hardened with additional light
3 exposure. The printed paste was dried in an oven at
4 150°C for a few minutes and fired in air in a BTU model
5 TFF 142-790A24 belt furnace with a temperature profile
6 as recommended by the paste manufacturer. The maximum
7 processing temperature was 850°C. The resulting
8 thickness of the fired electrode conductor layer was
9 about 9 microns.

10 A dielectric layer was formed on this
11 electrode layer as follows. A dielectric paste
12 comprising barium titanate (ESL # 4520 - available from
13 Electroscience Laboratories, King of Prussia,
14 Pennsylvania, dielectric constant 2500 - 3000) was
15 printed through a 200 mesh screen in a square pattern so
16 that all but an electrical contact pad at the edge of
17 the electrode was covered. The printed dielectric paste
18 was fired in air in the BTU furnace with a temperature
19 profile as recommended by the manufacturer (maximum
20 temperature 900 - 1000°C). The thickness of the
21 resulting fired dielectric was in the range of 12 to 15
22 microns. A second and third layer of the dielectric
23 were then printed and fired over the first layer in the
24 same manner. The combined thickness of the three
25 printed and sintered dielectric layers was 40 to 50
26 microns.

27 A phosphor layer was deposited directly onto
28 the dielectric layer in accordance with known thin film
29 techniques. In particular, a 0.5 micron thick layer of
30 zinc sulphide doped with 1 mole percent of manganese was
31 evaporated onto the dielectric layer using a UHV
32 Instruments Model 6000 electron beam evaporator. The
33 layers were heated under vacuum in the evaporator and
34 were held at a temperature of 150°C during the
35 evaporation process which took approximately 2 minutes.

36 The phosphor layer was coated with a 0.5
37 micron layer of a transparent electrical conductor
38 consisting of indium tin oxide. This layer was applied

1 by known thin film deposition techniques, in particular
2 using the electron beam evaporator at 400°C under vacuum.

3 The laminate was subsequently annealed in air
4 for 15 minutes at 450°C to anneal the phosphor and indium
5 tin oxide conductor layers. An indium solder contact
6 was provided to the ITO layer. The device was sealed
7 with a silicone sealant (Silicone Resin Clear Lacquer,
8 cat.#419, from M.G. Chemicals).

9 The device was tested by applying a DC voltage
10 of 200 volts across the two electrodes. The device was
11 observed to fail upon application of the voltage due to
12 electrical breakdown of the dielectric layer in the
13 region immediately surrounding the contact to the indium
14 tin oxide.

15 Without being bound by same, it is believed
16 that the failure of the device was because the
17 dielectric layer did not provide the needed smooth
18 surface for the phosphor layer. Microcracks could be
19 observed at the surface. This may, however, be due to
20 the presence of deleterious materials in the commercial
21 dielectric paste and is thus not an indication that
22 barium titanate cannot be used as a single or first
23 dielectric layer in accordance with the present
24 invention.

25 EXAMPLE 2

26 This example is included to illustrate that a
27 screen printed dielectric layer from a paste containing
28 lead niobate, a material known to have a high dielectric
29 constant and a lower sintering temperature than barium
30 titanate, provides adequate dielectric strength, but
31 does not luminesce.

32 A device was constructed that was similar to
33 that in Example 1, but having a dielectric layer formed
34 from a dielectric paste of lead niobate, Cermalloy #
35 IP9333 (dielectric constant about 3500, thickness as in
36 Example 1). The device, when tested was not subject to
37 dielectric breakdown when a DC voltage of 400 volts was
38 applied. However, it failed to luminesce on application
39 of an AC voltage.

Without being bound by the same it is believed that the failure to luminesce was due to compatibility problems at the interface with the phosphor layer. Thus this example should not be taken as an indication that lead niobate cannot be used as single or first dielectric layer in accordance with the present invention.

EXAMPLE 3

This example illustrates a two layer dielectric constructed in accordance with the present invention, with a first dielectric layer of lead niobate (as in Example 2) and a second dielectric layer of lead zirconate titanate. Favourable luminescence was achieved.

A device identical to that in Example 2 was constructed, but with the additional step of applying a layer of lead zirconate titanate (PZT) using a sol gel process to the printed and fired dielectric layer before the phosphor layer was applied. The sol was prepared in the following manner. Acetic acid was dehydrated at 105°C for 5 minutes. Twelve grams of lead acetate was dissolved into 7 ml. of the dehydrated acid at 80°C to form a colourless solution. The solution was allowed to cool, and 5.54 g of zirconium propoxide was stirred into the solution to form a pale yellow solution. The solution was held at 60°C to 80°C for five minutes after which 2.18 g of titanium isopropoxide was added with stirring. The resulting solution was agitated for approximately 20 minutes in an ultrasonic bath to ensure that any remaining solids were dissolved. Then, approximately 1.75 ml of a 4:2:1 ethylene glycol to propanol to water solution was added to make a stable sol. More ethylene glycol was added before coating to adjust the viscosity to the desired value for spin coating or dipping. The prepared dielectric layer was spin coated in one case and dipped in another case with the sol. In the case of spin coating the sol was dribbled onto the first dielectric layer which was spinning in a horizontal plane at 3000 rpm. In the case

1 of dipping, a higher viscosity sol was used. For the
2 dipping procedure the substrate was pulled from the sol
3 at a rate of 5 cm per minute. The resulting coated
4 assembly was then heated in air in an oven at a
5 temperature of 600°C for 30 minutes to convert the sol to
6 PZT. The thickness of the PZT layer was approximately
7 2 to 3 microns. The surface of the PZT layer was
8 observed to be considerably smoother than that of the
9 screen printed and sintered first dielectric layer.

10 Following application of the PZT layer, the
11 phosphor and transparent conductor layers were deposited
12 as in Example 1.

13 The completed laminate performed well with
14 luminosity versus voltage characteristics similar to or
15 better than those reported by Miyata et al. The
16 threshold voltage for minimum luminance for the display
17 was 110 V. Luminosity at 50 volts above threshold (i.e.
18 160 volts, 60 Hz) was 57 foot Lamberts.

19 EXAMPLE 4

20 This example is included to illustrate that
21 variations in the thickness of the dielectric layer have
22 an effect on both the operating voltage and the
23 luminance of the displays.

24 A display was constructed as in Example 3,
25 except that only two instead of three screen printed
26 layers of dielectric were applied. The thickness of the
27 first dielectric layer was correspondingly reduced to 25
28 to 30 microns.

29 The display functioned well. The threshold
30 voltage for minimum luminance was 70 volts (cp 110 volts
31 in Example 3), expected from theoretical considerations.
32 The luminosity at 50 volts above the threshold value
33 also decreased to 35 foot Lamberts (cp 57 foot Lamberts
34 in Example 3).

35 Example 5

36 This example illustrates the preferred
37 embodiment of connecting the row and column address
38 lines of the EL laminate to the driver circuit using
39 through holes.

1 An addressable EL display was constructed
2 using the same sequence of layer depositions as set
3 forth in Example 3. The substrate was a 0.025 inch
4 thick rectangle of alumina obtained from Coors Ceramics
5 (Grand Junction, Colorado, U.S.A.) having dimensions of
6 length - 6 inches and width - 2 inches. The substrate
7 was drilled with 0.006 inch diameter through holes using
8 a carbon dioxide laser in the pattern shown in Figure 4.
9 The substrate was inspected to ensure that all of the
10 holes were clear. The holes were found to be about
11 0.008 inches in diameter on the side facing the laser
12 and about 0.006 inches on the opposite side. The side
13 with the wider hole openings was chosen to be the rear
14 side of the substrate to facilitate flowing conductive
15 material into the through holes.

16 Following this, the circuit pattern shown in
17 Figure 5 was printed onto the rear side of the substrate
18 through a 325 mesh stainless steel screen using
19 Cermalloy #4740 silver platinum paste. During the
20 printing process, the substrate was aligned with a
21 master plate having 0.040 inch holes drilled in the same
22 pattern as shown in Figure 4 and a vacuum was applied
23 below the master plate to pull the conductive paste
24 through the through holes in the substrate (i.e. through
25 to the front, viewing side of the substrate). This step
26 formed the circuit pattern of Figure 5 together with a
27 conductive path through each of the through holes in the
28 substrate. To ensure uniformity in the application of
29 the vacuum, the vacuum was not turned on until the
30 substrate had been printed. The part was inspected to
31 ensure that the through holes were filled.

32 Following printing, the substrate was fired in
33 air in a BTU model TFF 142-790A24 belt furnace with a
34 temperature profile recommended by the paste
35 manufacturer. The maximum temperature was 850°C.

36 Following this step, a circuit reinforcement
37 pattern as shown in Figure 7 was printed and fired on
38 the rear, circuit side of the substrate (using the same
39 Cermalloy conductive paste). This step made the circuit

1 pattern thicker in certain areas where electrical
2 connections were to be subsequently made.

3 The row address lines and the front row and
4 column connector pads were then screen printed on the
5 front viewing side of the substrate. The lines extended
6 across the length of the substrate to the row connector
7 pads in the pattern shown in Figure 6. The column
8 connector pads, as shown in Figure 6, were printed in
9 this same step. The row address lines and connector
10 pads were formed from the same conductive paste
11 (Cermalloy #4740) using the same printing and firing
12 conditions. The substrate was positioned on the same
13 master plate with the through hole pattern of Figure 4
14 and a vacuum was applied from below to pull the
15 conductive paste through the through holes toward the
16 rear side of the substrate. The thickness of the fired
17 electrode layer was about 8 micrometers. There were
18 about 52 address lines per inch and the total number of
19 address lines was 68. The part was examined to ensure
20 the through holes were filled.

21 The three layers of the dielectric paste
22 (Cermalloy #IP9333) were printed and fired as set forth
23 in Example 3 to form a dielectric layer of about 50
24 micrometers thickness.

25 The rear, circuit side of the substrate was
26 then sealed. A thick film glass paste (Heraeus IP9028,
27 from Heraeus-Cermalloy, Conshohocken, Pa.) was screen
28 printed using a 250 mesh screen in the pattern shown in
29 Figure 8. The connector pads for connection to the high
30 voltage driver chips and other driver circuitry were
31 left uncovered. The glass sealing layer was then fired
32 in the BTU belt furnace using a temperature profile
33 recommended by the manufacturer with a maximum
34 temperature of 700°C.

35 During the above mentioned firing steps, the
36 substrate was supported on pieces of ceramic material at
37 either end to avoid contact between the printed material
38 on the circuit side and the belt of the furnace.

1 The sol gel layers were then formed by dipping
2 substantially as set out in Example 3. Three or four
3 sol gel layers were typically used, with pulling rates
4 of 10 - 25 sec/in from a mixture having a viscosity of
5 about 100 cp as measured by the falling ball viscometer.
6 Between dipping layers, the sol gel was dried at 110°C
7 for 10 min. A vacuum chuck was placed over the active
8 area of the laminate and the sol gel was water washed
9 off the remaining areas. The layer was then fired at
10 about 600°C in a belt furnace for 25 min. A total sol
11 gel thickness between 3 - 10 micrometres was achieved.
12 This was followed by the phosphor layer of Example 3
13 using zinc sulfide doped with 1% manganese with a
14 thickness of 0.5 - 1.0 micrometers.

15 The column address lines were then deposited
16 from indium tin oxide, as described in Example 3, in the
17 pattern shown in Figure 9. There were about 52 column
18 address lines per inch and a total of 256 columns. The
19 spacing between the lines was 0.001 inches and the line
20 width was 0.019 inches (center to center).

21 Silver was evaporated through a shadow mask in
22 the pattern shown in Figure 10 to make the electrical
23 connections of the column address lines to the column
24 connector pads and through hole conductors on the
25 substrate.

26 The viewing surface of the laminate was sealed
27 with a silicone sealant sprayed over the entire front
28 face of the display. The sealant used was Silicone
29 Resin Clear Lacquer, Cat. #419 from M.G. Chemicals.

30 The completed display was tested by connecting
31 a pulse generator providing a 160V square wave signal at
32 60 Hz across pairs of row and column pads on the circuit
33 deposited on the rear of the substrate. Each pixel of
34 the display was found to light up independently and with
35 a consistent intensity equal to that measured in Example
36 3 when the voltage was applied. No dysfunctional pixels
37 were found among the total pixel count of 17408.

1 EXAMPLE 6

2 This example illustrates the preferred
3 embodiment of laser scribing the indium tin oxide
4 address lines of the EL laminate of the present
5 invention.

6 An addressable matrix display was constructed
7 on a ceramic substrate using the following procedure.
8 The substrate was a 0.025 inch thick rectangle of
9 alumina with length 6 inches and width 2 inches obtained
10 from Coors Ceramics (Grand Junction, Colorado, U.S.A.).
11 This was drilled with 0.006 inch diameter holes with a
12 carbon dioxide laser in the pattern shown in Figure 4.
13 The part was inspected to ensure that all of the holes
14 were clear.

15 Following this step, the circuit pattern shown
16 in Figure 5 was printed through a 325 mesh stainless
17 steel screen using Cermalloy (Conshohocken Pennsylvania,
18 U.S.A.) #4740 silver platinum paste. During the
19 printing process, the substrate was aligned with a
20 master plate having 0.040 inch holes drilled in the same
21 pattern as the substrate to facilitate applying a vacuum
22 to the substrate holes during printing. The vacuum
23 sucked paste through the holes to facilitate the
24 formation of a conductive path through the ceramic
25 substrate after the part was fired. The part was fired
26 in air in a BTU model TFF 142-790A24 belt furnace with
27 a temperature profile recommended by the paste
28 manufacturer, having a maximum temperature of 850°C.

29 Following this step, a circuit reinforcement
30 pattern as shown in Figure 7 was printed and fired on
31 the rear, circuit side of the substrate (using the same
32 Cermalloy conductive paste). This step made the circuit
33 pattern thicker in certain areas where electrical
34 connections were to be subsequently made.

35 Following this, a set of row address lines and
36 connector pads were printed on the front viewing side of
37 the substrate. The lines extended along the length of
38 the substrate to the row connector pads (as shown in
39 Figure 6). The column connector pads were also formed

1 in this step (as shown in Figure 6). The row address
2 lines and the row and column connector pads were formed
3 from the same silver platinum paste using the same
4 printing and firing conditions. The substrate was
5 positioned on the same master plate with the through
6 hole pattern of Figure 4 and a vacuum was applied from
7 below to pull the conductive paste through the through
8 holes toward the rear side of the substrate. The
9 thickness of the fired electrode layer was about 8
10 micrometers. There were 52 address lines per inch and
11 the total number of address lines was 68.

12 Next three layers of lead niobate dielectric
13 paste (Cermalloy #IP9333) were sequentially printed and
14 fired in the belt furnace with a temperature profile as
15 recommended by the manufacturer (maximum temperature
16 850C) on top of the row address lines (as set forth in
17 Example 3). The combined thickness of the dielectric
18 layers was 50 micrometers.

19 Following this, the rear, circuit side of the
20 substrate was sealed as set forth in Example 5, in the
21 pattern shown in Figure 8.

22 Next, a 3 - 10 micrometer thick layer of lead
23 zirconate titanate (PZT) was deposited on the lead
24 niobate layer to form a smooth surface. The sol gel
25 technique using dipping, as set out in Example 5, was
26 used. A thin film phosphor layer was then deposited
27 using electron beam evaporation methods as known in the
28 art. The phosphor layer was zinc sulfide doped with 1%
29 manganese, which was deposited to a thickness of between
30 0.5 and 1 micrometers.

31 The next step was to deposit a 300 nanometre
32 thick layer of indium tin oxide (ITO) on the phosphor
33 layers using electron beam evaporation methods as known
34 in the art.

35 This ITO layer was then patterned into 256
36 address lines using a 2 Watt CW (continuous wave) argon
37 ion laser tuned to a wavelength of 514.5 nanometres.
38 The EL laminate was mounted on a moveable X coordinate
39 table, which moved the laminate in a direction

1 perpendicular to the lines being scribed beneath the
2 laser beam. The laser beam was moved in the Y direction
3 to scribe the lines. The laser beam was focussed to a
4 12 micrometer spot and the laser power was adjusted so
5 that the indium tin oxide, the underlying phosphor layer
6 and about 10% of the combined underlying dielectric
7 layers were ablated away where the laser beam had
8 scanned (about 1.8 W). The scanning speed was
9 controlled at about 100 and 500 mm/sec to provide
10 address lines with about 40 or 25 micrometres gap
11 respectively and address line depth of 6-8 or 3-4
12 micrometres respectively. The spacing between address
13 lines (i.e. between centres of the lines) was about 500
14 micrometers. A vacuum adjacent the substrate withdrew
15 vaporized and ablated material. The pattern of the
16 transparent electrodes, once the ablation was completed,
17 was as shown in Figure 9. On the completed display,
18 there were about 50 column address lines per inch and a
19 total of 256 columns.

20 Prior to scribing the ITO column address
21 lines, the silver interconnects between the front
22 (column) connector pads and the ultimate ITO address
23 lines were screen printed from silver through a shadow
24 mask in the pattern of Figure 10.

25 After laser scribing, the front viewing side
26 of the completed display was sprayed with a protective
27 polymer coating (Silicone Resin Clear Lacquer, cat #419
28 from MG Chemicals).

29 The display was then tested by applying a
30 voltage across selected pixels by connecting a pulsed
31 power supply providing voltage pulses of 160 volts at a
32 repetition rate of 64 Hz. The pixels each lit up
33 reliably with a luminosity similar to that of the single
34 pixel device of the previous example.

35 The resolution of the address lines of this
36 example is generally much higher than is achievable with
37 state of the art photolithographic techniques.

1 Commercially available devices typically have ITO
2 address lines with widths of 180 - 205 micrometers and
3 gaps between the lines of 65 - 80 micrometers. As set
4 out above, in accordance with this invention, gaps of 25
5 and 40 micrometers were produced, depending on the laser
6 scanning speed. This higher resolution allows for a
7 higher ratio of active to total area of the display,
8 since wider ITO address lines with smaller gaps can be
9 used.

10 **EXAMPLE 7**

11 This example illustrates a two layer
12 dielectric constructed in accordance with the present
13 invention but with the first dielectric layer being
14 constructed from a paste having a higher dielectric
15 constant than the paste used in Examples 3 and 4.

16 The device was constructed as set forth in
17 Example 3, but having a first dielectric layer formed
18 from a lead niobate paste available from Electroscience
19 Laboratories as a high K capacitor paste under the
20 number 4210. The sintered paste has a dielectric
21 constant of about 10,000. The first dielectric layer
22 had a thickness of about 50 microns. A sol gel layer of
23 PZT was applied, as described in Example 3, to a
24 thickness of about 5 microns.

25 The device functioned well with a threshold
26 voltage for minimum luminance of 91 Volts and a
27 luminosity at 150 Volts of 50 foot Lamberts.

28 **EXAMPLE 8**

29 This example illustrates a two layer
30 dielectric constructed with a first dielectric layer
31 formed from a lead niobate paste and a second dielectric
32 layer formed from lead lanthanum zirconate titanate
33 (PLZT). PLZT has a dielectric constant of about 1,000.
34 The PLZT had a molar ratio of zirconium to titanium to
35 lanthanum of 52:32:16.

1 The device was constructed as set forth in
2 Example 3, with the sol gel layer being prepared as
3 follows:

4 Into 50 ml of glacial acetic acid was
5 dissolved 120 grams of 99.5% purity lead acetate. The
6 resulting solution was heated to 90°C and held at this
7 temperature for 2 minutes before being cooled to 70°C.
8 Next, 55.4 grams of zirconium propoxide was added and
9 the resulting solution was heated to 80°C and held at
10 that temperature for 1 minute. After cooling to 70°C,
11 21.8 grams of titanium isopropoxide was added. Next,
12 11.4 grams of lanthanum nitrate was dissolved in 20 ml
13 of glacial acetic acid, and this was added to the
14 solution. Finally, to stabilize the solution and adjust
15 the viscosity to a suitable value, 10 ml of ethylene
16 glycol, 5 ml of propan-2-ol and 2.5 ml of demineralized
17 water were added.

18 The PLZT sol gel was applied to the first
19 dielectric layer by dipping in a manner similar to that
20 described in Example 3. The dipped parts were fired at
21 600°C to convert the second layer to PLZT. Four coats of
22 PLZT were applied by successive dipping and firing in
23 this way to prepare a surface of adequate smoothness for
24 the deposition of the phosphor layer. A total thickness
25 of 5 microns was achieved.

26 The device functioned well with a threshold
27 voltage of 75 Volts and a luminosity of 37 foot Lamberts
28 at 150 Volts.

29 All publications mentioned in this
30 specification are indicative of the level of skill of
31 those skilled in the art to which this invention
32 pertains. All publications are herein incorporated by
33 reference to the same extent as if each individual
34 publication was specifically and individually indicated
35 to be incorporated by reference.

36 The terms and expressions used in this
37 specification are used as terms of description and not

1 of limitation. There is no intention, in using such
2 terms and expressions, of excluding equivalents of the
3 features shown and described, it being recognized that
4 the scope of the invention is defined and limited only
5 by the claims which follow.

1 CLAIMS:

2 1. A dielectric layer in an
3 electroluminescent laminate of the type including a
4 phosphor layer sandwiched between a front and a rear
5 electrode, the rear electrode being formed on a
6 substrate and the phosphor layer being separated from
7 the rear electrode by a dielectric layer, the dielectric
8 layer comprising:

9 a planar layer formed from a ceramic
10 material providing a dielectric strength greater than
11 about 1.0×10^6 V/m and a dielectric constant such that
12 the ratio of the dielectric constant of the dielectric
13 material to that of the phosphor is greater than about
14 50:1, the dielectric layer having a thickness such that
15 the ratio of the thickness of the dielectric layer to
16 that of the phosphor layer is in the range of about 20:1
17 to 500:1, and the dielectric layer having a surface
18 adjacent the phosphor layer which is compatible with the
19 phosphor layer and sufficiently smooth that the phosphor
20 layer illuminates generally uniformly at a given
21 excitation voltage.

22 2. The dielectric layer as set forth in
23 claim 1, wherein the ratio of the dielectric constant of
24 the dielectric material to that of the phosphor material
25 is greater than about 100:1, and wherein the dielectric
26 layer has a thickness such that the ratio of the
27 thickness of the dielectric layer to that of the
28 phosphor layer is in the range of about 40:1 to 300:1.

29 3. The dielectric layer as set forth in
30 claim 1 in an electroluminescent laminate of the type
31 including a thin film phosphor layer sandwiched between
32 a front, transparent electrode and a rear electrode and
33 separated from the rear electrode by the dielectric
34 layer.

35 4. The dielectric layer as set forth in
36 claim 3, having a dielectric constant greater than about

1 500 and a thickness in the range of about 10 - 300
2 microns.

3 5. The dielectric layer as set forth in
4 claim 4, formed from at least two layers, a first
5 dielectric layer formed on the rear electrode and having
6 the dielectric strength and dielectric constant values
7 as set forth in claim 4, and a second dielectric layer
8 formed on the first dielectric layer and having the
9 surface adjacent the phosphor layer as set forth in
10 claim 1, the first and second dielectric layers having
11 a combined thickness as set forth in claim 4.

12 6. The dielectric layer as set forth in
13 claim 5, wherein the first and second dielectric layers
14 are formed from ferroelectric ceramic materials.

15 7. The dielectric layer as set forth in
16 claim 5, wherein the second dielectric layer provides a
17 dielectric constant of at least 20 and a thickness of at
18 least about 2 microns.

19 8. The dielectric layer as set forth in
20 claim 7, wherein the first dielectric layer provides a
21 dielectric constant of at least 1000 and the second
22 dielectric layer provides a dielectric constant of at
23 least 100.

24 9. The dielectric layer as set forth in
25 claim 8, wherein the first dielectric layer has a
26 thickness in the range of about 20 -150 microns and the
27 second dielectric layer has a thickness in the range of
28 about 2 - 10 microns.

29 10. The dielectric layer as set forth in
30 claim 9, wherein the first and second dielectric layers
31 are formed from ferroelectric ceramic materials having
32 perovskite crystal structures.

33 11. The dielectric layer as set forth in
34 claim 5, 6 or 10, wherein the first dielectric layer is
35 formed by thick film techniques followed by sintering at
36 a temperature less than the melting point of the rear
37 electrode.

1 12. The dielectric layer as set forth in
2 claim 11, wherein the first dielectric layer is formed
3 by screen printing.

4 13. The dielectric layer as set forth in
5 claim 11, wherein the second dielectric layer is formed
6 by sol gel techniques followed by sintering at a
7 temperature less than the melting point of the rear
8 electrode.

9 14. The dielectric layer as set forth in
10 claim 12, wherein the second dielectric layer is formed
11 by sol gel techniques, including spin deposition or
12 dipping followed by sintering at a temperature less than
13 the melting point of the rear electrode.

14 15. The dielectric layer as set forth in
15 claim 5, 6, or 10, wherein the first dielectric layer is
16 formed from lead niobate and wherein the second
17 dielectric layer is formed from lead zirconate titanate
18 or lead lanthanum zirconate titanate.

19 16. The dielectric layer as set forth in
20 claim 11, wherein the first dielectric layer is formed
21 from lead niobate and wherein the second dielectric
22 layer is formed from lead zirconate titanate or lead
23 lanthanum zirconate titanate.

24 17. The dielectric layer as set forth in
25 claim 14, wherein the first dielectric layer is formed
26 from lead niobate and wherein the second dielectric
27 layer is formed from lead zirconate titanate or lead
28 lanthanum zirconate titanate.

29 18. The dielectric layer as set forth in
30 claim 14 in a laminate having the rear electrode formed
31 on a substrate which can withstand the sintering
32 temperature.

33 19. The dielectric layer as set forth in
34 claim 18, wherein the substrate is alumina.

35 20. The dielectric layer as set forth in
36 claim 4, 5 or 14, wherein the surface of the dielectric
37 layer adjacent the phosphor layer has a surface relief

1 which does not vary more than about 0.5 microns over
2 about 1000 microns.

3 21. The dielectric layer as set forth in
4 claim 17 in a laminate having the rear electrode formed
5 of silver/platinum address lines on an alumina substrate
6 and the front electrode formed of indium tin oxide
7 address lines.

8 22. The dielectric layer as set forth in
9 claim 21 in a laminate having a sealing layer above the
10 front electrode.

11 23. A method of forming a dielectric layer in
12 an electroluminescent laminate of the type including a
13 phosphor layer sandwiched between a front and a rear
14 electrode, the rear electrode being formed on a
15 substrate and the phosphor layer being separated from
16 the rear electrode by a dielectric layer, comprising:

17 depositing on the rear electrode, by
18 thick film techniques followed by sintering, a ceramic
19 material having a dielectric constant such that the
20 ratio of the dielectric constant of the dielectric
21 material to that of the phosphor material is greater
22 than about 50:1, to form a dielectric layer having a
23 dielectric strength greater than about 1.0×10^6 V/m and
24 a thickness such that the ratio of the thickness of the
25 dielectric layer to that of the phosphor layer is in the
26 range of about 20:1 to 500:1, the dielectric layer
27 forming a surface adjacent the phosphor layer which is
28 compatible with the electroluminescent layer and
29 sufficiently smooth that the phosphor layer illuminates
30 generally uniformly at a given excitation voltage.

31 24. The method as set forth in claim 23,
32 wherein the ratio of the dielectric constant of the
33 dielectric material to that of the phosphor material is
34 greater than about 100:1, and wherein the ratio of the
35 thickness of the dielectric layer to that of the
36 phosphor layer is in the range of about 40:1 to 300:1.

1 25. The method as set forth in claim 23,
2 wherein the dielectric layer is formed in an
3 electroluminescent laminate of the type including a thin
4 film phosphor layer sandwiched between a front,
5 transparent electrode and a rear electrode and separated
6 from the rear electrode by the dielectric layer.

7 26. The method as set forth in claim 25,
8 wherein the dielectric constant of the ceramic material
9 is greater than about 500 and the thickness of the
10 dielectric layer is in the range of about 10 - 300
11 microns.

12 27. The method as set forth in claim 26,
13 wherein the dielectric layer is formed as at least two
14 layers, a first dielectric layer which is deposited on
15 the rear electrode by thick film techniques and having
16 the dielectric strength and dielectric constant values
17 as set forth in claim 26, and a second dielectric layer
18 which is deposited on the second dielectric layer to
19 provide the surface adjacent the phosphor layer as set
20 forth in claim 23, the first and second dielectric
21 layers having a combined thickness as set forth in claim
22 26.

23 28. The method as set forth in claim 27,
24 wherein the first and second dielectric layers are
25 formed from ferroelectric ceramic materials.

26 29. The method as set forth in claim 27,
27 wherein the second dielectric layer provides a
28 dielectric constant of at least 20 and a thickness of at
29 least about 2 microns.

30 30. The method as set forth in claim 29,
31 wherein the first dielectric layer provides a dielectric
32 constant of at least 1000 and the second dielectric
33 layer provides a dielectric constant of at least 100.

34 31. The dielectric layer as set forth in
35 claim 30, wherein the first dielectric layer has a
36 thickness in the range of about 20 - 150 microns and the

1 second dielectric layer has a thickness in the range of
2 about 2 - 10 microns.

3 32. The dielectric layer as set forth in
4 claim 31, wherein the first and second dielectric layers
5 are formed from ferroelectric ceramic materials having
6 perovskite crystal structures.

7 33. The method as set forth in claim 27, 28
8 or 32, wherein the first dielectric layer is deposited
9 by thick film techniques followed by sintering at a
10 temperature less than the melting point of the rear
11 electrode.

12 34. The method as set forth in claim 33,
13 wherein the first dielectric layer is deposited by
14 screen printing.

15 35. The method as set forth in claim 33,
16 wherein the second dielectric layer is deposited by sol
17 gel techniques followed by sintering at a temperature
18 less than the melting point of the rear electrode.

19 36. The method as set forth in claim 34,
20 wherein the second dielectric layer is deposited by sol
21 gel techniques, including spin deposition or dipping,
22 followed by sintering at a temperature less than the
23 melting point of the rear electrode.

24 37. The method as set forth in claim 27, 28,
25 or 32, wherein the first dielectric layer is formed from
26 lead niobate and wherein the second dielectric layer is
27 formed from lead zirconate titanate or lead lanthanum
28 zirconate titanate.

29 38. The method as set forth in claim 33,
30 wherein the first dielectric layer is formed from lead
31 niobate and wherein the second dielectric layer is
32 formed from lead zirconate titanate or lead lanthanum
33 zirconate titanate.

34 39. The method as set forth in claim 36,
35 wherein the first dielectric layer is formed from lead
36 niobate and wherein the second dielectric layer is

1 formed from lead zirconate titanate or lead lanthanum
2 zirconate titanate.

3 40. The method as set forth in claim 36,
4 wherein the dielectric layer is formed in a laminate
5 having the rear electrode formed on a substrate which
6 can withstand the sintering temperature.

7 41. The method as set forth in claim 40,
8 wherein the substrate is alumina.

9 42. The method as set forth in claim 26, 27,
10 or 36, wherein the surface of the dielectric layer
11 adjacent the phosphor layer has a surface relief which
12 does not vary more than about 0.5 microns over about
13 1000 microns.

14 43. The method as set forth in claim 39,
15 wherein the dielectric layer is formed in a laminate
16 having the rear electrode formed of silver/platinum
17 address lines on an alumina substrate and the front
18 electrode formed of indium tin oxide address lines.

19 44. The method as set forth in claim 43,
20 wherein the dielectric layer is formed in a laminate
21 having a sealing layer above the front electrode.

22 45. An electroluminescent display panel
23 providing for electrical connection from a planar
24 electroluminescent laminate to voltage driving
25 circuitry, comprising:

26 a phosphor layer sandwiched between a
27 front and a rear set of intersecting address lines, the
28 rear address lines being formed on a substrate and the
29 phosphor layer being separated from the rear address
30 lines and optionally from the front address lines, by a
31 dielectric layer;

32 said substrate forming a plurality of
33 through holes;

34 means forming a conductive path through
35 each of the through holes in the substrate to each of
36 the address lines for providing for electrical

1 connection of each address line to the voltage driving
2 circuit.

3 46. The display panel as set forth in claim
4 45, wherein the voltage driving circuit includes voltage
5 driver components, the outputs of which are connected to
6 the address lines through the through holes, the voltage
7 driver components being mounted on the rear of the
8 substrate.

9 47. The display panel as set forth in claim
10 46, wherein the means forming the conductive path
11 comprises:

12 a conductive material deposited in each
13 of the through holes forming front and rear connector
14 pads on each side of the substrate; and

15 conductive material between the front
16 connector pads and each of the address lines.

17 48. The display panel as set forth in Claim
18 47, wherein the substrate is formed from a material
19 which can withstand temperatures of about 850°C.

20 49. The display panel as set forth in Claim
21 48, wherein the substrate is opaque.

22 50. The display panel as set forth in Claim
23 48, wherein the substrate is alumina.

24 51. The display panel as set forth in claim
25 47, wherein the substrate is generally rectangular and
26 wherein the holes are formed around the perimeter of the
27 substrate adjacent the ends of the address lines on at
28 least two sides.

29 52. The display as set forth in claim 51,
30 wherein the conductive material is a fired thick film
31 paste.

32 53. The display as set forth in claim 52,
33 wherein the conductive material to the rear address
34 lines is silver/platinum and the conductive material to
35 the front address lines is silver.

1 54. The display as set forth in claim 46,
2 wherein the means forming the conductive path through
3 each of the through holes comprises:

4 a first fired thick film conductive
5 paste printed in a circuit pattern on the rear of the
6 substrate and pulled through the holes in the substrate
7 to provide front and rear connector pads, said rear
8 connector pads providing for electrical connection to
9 the voltage driving circuit; and

10 a second fired conductive paste between
11 the front connector pads and the address lines.

12 55. The display as set forth in claim 54,
13 wherein the voltage driving circuit includes voltage
14 driving components and wherein the circuit pattern
15 provides further connector pads for electrical
16 connection for the outputs of the voltage driving
17 components and to the drive circuit.

18 56. The display as set forth in claim 55,
19 wherein the substrate is generally rectangular and
20 wherein the holes are formed around the perimeter of the
21 substrate adjacent the ends of the address lines on at
22 least two sides.

23 57. The display as set forth in claim 56,
24 wherein the first thick film paste is a silver platinum
25 paste and the second thick film paste is a silver paste.

26 58. The display as set forth in claim 54,
27 wherein the dielectric layer comprises:

28 a planar layer formed from a ceramic
29 material providing a dielectric strength greater than
30 about 1.0×10^6 V/m and a dielectric constant such that
31 the ratio of the dielectric constant of the dielectric
32 material to that of the phosphor is greater than about
33 50:1, the dielectric layer having a thickness such that
34 the ratio of the thickness of the dielectric layer to
35 that of the phosphor layer is in the range of about 20:1
36 to 500:1, and the dielectric layer having a surface
37 adjacent the phosphor layer which is compatible with the

1 phosphor layer and sufficiently smooth that the phosphor
2 layer illuminates generally uniformly at a given
3 excitation voltage.

4 59. The display as set forth in claim 58,
5 wherein the dielectric layer is formed from at least two
6 layers, a first dielectric layer formed on the rear
7 electrode and having a dielectric constant greater than
8 about 500 and a thickness in the range of about 10 to
9 300 microns, and a second dielectric layer formed on the
10 first dielectric layer and having the surface adjacent
11 the phosphor layer as set forth in claim 58, the first
12 and second dielectric layers having a combined thickness
13 of about 10 to 300 microns.

14 60. The display as set forth in claim 59,
15 wherein the first and second dielectric layers are
16 formed from ferroelectric ceramic materials having
17 perovskite crystal structures, wherein the first
18 dielectric layer provides a dielectric constant of at
19 least 1000 and has a thickness of about 20 - 150
20 microns, and wherein the second dielectric layer
21 provides a dielectric constant of at least 100 and has
22 a thickness of about 2 - 10 microns.

23 61. The display as set forth in claim 60,
24 wherein the first dielectric layer is formed by screen
25 printing and sintering a thick film dielectric paste and
26 the second dielectric layer is formed by sol gel
27 techniques followed by firing.

28 62. The display as set forth in claim 61,
29 wherein the first dielectric layer is formed from lead
30 niobate and wherein the second dielectric layer is
31 formed from lead zirconate titanate or lead lanthanum
32 zirconate titanate.

33 63. A process for laser scribing a pattern in
34 a planar laminate having at least one overlying layer
35 and at least one underlying layer, comprising:

36 applying a focussed laser beam on the
37 overlying layer side of the laminate, said laser beam

1 having a wavelength which is substantially unabsorbed by
2 the overlying layer but which is absorbed by the
3 underlying layer, such that at least a portion of the
4 underlying layer is directly ablated and the overlying
5 layer is indirectly ablated throughout its thickness.

6 64. The process of claim 63, wherein the
7 overlying layer is transparent to visible light and the
8 underlying layer is opaque to visible light and wherein
9 the wavelength of the laser beam is in the visible or
10 infrared region of the electromagnetic spectrum.

11 65. The process of claim 63, wherein the
12 composition and thicknesses of the layers are such that:

13 $\sum_i \alpha_{v_i} T_{v_i} > \sum_i \alpha_{o_i} T_{o_i}$
14 wherein;
15 α_v = absorption coefficient of underlying layer;
16 α_o = absorption coefficient of overlying layer;
17 T_v = thickness of underlying layer; and
18 T_o = thickness of overlying layer.

19 66. The process of claim 65, wherein the
20 composition of the layers is such that the overlying
21 layer vaporizes at a lower temperature than does the
22 underlying layer.

23 67. The process of claim 66, wherein the
24 composition of the layers is such that the overlying
25 layer has a higher thermal conductivity than does the
26 underlying layer.

27 68. The process of claim 63, wherein the
28 overlying layer is a transparent conductive material
29 into which an electrode pattern is scribed.

30 69. The process of claim 68, wherein the
31 electrode pattern is formed by moving one or both of the
32 laminate and the laser beam relative to the other.

33 70. The process of claim 69, wherein the
34 laminate is an EL laminate having overlying layers of a
35 transparent conductive material and phosphor and an
36 underlying layer of one or more dielectric layers and
37 wherein the electrode pattern consists of a plurality of

1 parallel spaced address lines of the transparent
2 conductive material.

3 71. The process of claim 70, wherein a
4 portion of the dielectric layer is directly ablated and
5 the phosphor and transparent conductive material are
6 indirectly ablated throughout their thicknesses.

7 72. The process of claim 71, wherein the
8 transparent conductive material is indium tin oxide.

9 73. The process of claim 72, wherein the
10 dielectric layer comprises:

11 a planar layer formed from a ceramic
12 material providing a dielectric strength greater than
13 about 1.0×10^6 V/m and a dielectric constant such that
14 the ratio of the dielectric constant of the dielectric
15 material to that of the phosphor is greater than about
16 50:1, the dielectric layer having a thickness such that
17 the ratio of the thickness of the dielectric layer to
18 that of the phosphor layer is in the range of about 20:1
19 to 500:1, and the dielectric layer having a surface
20 adjacent the phosphor layer which is compatible with the
21 phosphor layer and sufficiently smooth that the phosphor
22 layer illuminates generally uniformly at a given
23 excitation voltage.

24 74. The process as set forth in claim 73,
25 wherein the dielectric layer is formed from at least two
26 layers, a first dielectric layer formed on the rear
27 electrode and having a dielectric constant greater than
28 about 500 and a thickness in the range of about 10 to
29 300 microns, and a second dielectric layer formed on the
30 first dielectric layer and having the surface adjacent
31 the phosphor layer as set forth in claim 73, the first
32 and second dielectric layers having a combined thickness
33 of about 10 to 300 microns.

34 75. The process as set forth in claim 74,
35 wherein the first and second dielectric layers are
36 formed from ferroelectric ceramic materials having
37 perovskite crystal structures, wherein the first

1 dielectric layer provides a dielectric constant of at
2 least 1000 and has a thickness of about 20 - 150
3 microns, and wherein the second dielectric layer
4 provides a dielectric constant of at least 100 and has
5 a thickness of about 2 - 10 microns.

6 76. The process as set forth in claim 75,
7 wherein the first dielectric layer is formed by screen
8 printing and sintering a thick film dielectric paste and
9 the second dielectric layer is formed by sol gel
10 techniques followed by firing.

11 77. The process as set forth in claim 76,
12 wherein the first dielectric layer is formed from lead
13 niobate and wherein the second dielectric layer is
14 formed from lead zirconate titanate or lead lanthanum
15 zirconate titanate.

16 78. A process of forming an EL laminate
17 having a phosphor layer sandwiched between a front and
18 rear set of intersecting address lines, the rear address
19 lines being formed on a substrate and the phosphor layer
20 being separated from the rear address lines, and
21 optionally from the front address lines, by a dielectric
22 layer, comprising the steps of:

23 (a) forming the rear address lines on the
24 substrate;

25 (b) forming the dielectric layer on the rear
26 address lines;

27 (c) forming the phosphor layer on the
28 dielectric layer;

29 (d) optionally forming a transparent
30 dielectric layer on the phosphor layer; and then

31 (e) forming the front address lines on the
32 underlying phosphor or transparent dielectric layer by
33 depositing a layer of transparent conductive material on
34 the underlying layer and scribing the address lines
35 therein with a focused laser beam, said laser beam
36 having a wavelength which is substantially unabsorbed by
37 the transparent conductive material, the transparent

1 dielectric layer and the phosphor layer but which is
2 absorbed by the underlying dielectric layer, such that
3 a portion of the underlying dielectric layer is directly
4 ablated by the laser beam and the overlying phosphor,
5 optional transparent dielectric and transparent
6 conductive material are indirectly ablated throughout
7 their thicknesses.

8 79. The process of claim 78, wherein the
9 laser beam has a wavelength greater than about 400 nm.

10 80. The process of claim 79, wherein the
11 composition and thicknesses of the layers are such that:

12 $\sum_i \alpha_{d_i} T_{d_i} > \sum_i \alpha_t T_t$,
13 wherein:

14 α_d = absorption coefficient of underlying dielectric
15 layer

16 α_t = absorption coefficient of transparent layers

17 T_d = thickness of underlying dielectric layer

18 T_t = thickness of transparent layers.

19 81. The process of claim 80, wherein the
20 transparent conductive material is indium tin oxide.

21 82. The process of claim 81, wherein the
22 dielectric layer underlying the phosphor layer
23 comprises:
24

25 a planar layer formed from a ceramic
26 material providing a dielectric strength greater than
27 about 1.0×10^6 V/m and a dielectric constant such that
28 the ratio of the dielectric constant of the dielectric
29 material to that of the phosphor is greater than about
30 50:1, the dielectric layer having a thickness such that
31 the ratio of the thickness of the dielectric layer to
32 that of the phosphor layer is in the range of about 20:1
33 to 500:1, and the dielectric layer having a surface
34 adjacent the phosphor layer which is compatible with the
35 phosphor layer and sufficiently smooth that the phosphor
36 layer illuminates generally uniformly at a given
37 excitation voltage.

38 83. The process as set forth in claim 82,
39 wherein the dielectric layer is formed from at least two

1 layers, a first dielectric layer formed on the rear
2 electrode and having a dielectric constant greater than
3 about 500 and a thickness in the range of about 10 to
4 300 microns, and a second dielectric layer formed on the
5 first dielectric layer and having the surface adjacent
6 the phosphor layer as set forth in claim 82, the first
7 and second dielectric layers having a combined thickness
8 of about 10 to 300 microns.

9 84. The process as set forth in claim 83,
10 wherein the first and second dielectric layers are
11 formed from ferroelectric ceramic materials having
12 perovskite crystal structures, wherein the first
13 dielectric layer provides a dielectric constant of at
14 least 1000 and has a thickness of about 20 - 150
15 microns, and wherein the second dielectric layer
16 provides a dielectric constant of at least 100 and has
17 a thickness of about 2 - 10 microns.

18 85. The process as set forth in claim 84,
19 wherein the first dielectric layer is formed by screen
20 printing and sintering a thick film dielectric paste and
21 the second dielectric layer is formed by sol gel
22 techniques followed by firing.

23 86. The process as set forth in claim 85,
24 wherein the first dielectric layer is formed from lead
25 niobate and wherein the second dielectric layer is
26 formed from lead zirconate titanate or lead lanthanum
27 zirconate titanate.

28 87. An EL laminate comprising:
29 a rear substrate;
30 a rear set of parallel spaced address lines on
31 the rear substrate;
32 a dielectric layer on the rear address lines;
33 a phosphor layer on the dielectric layer;
34 an optional transparent dielectric layer on
35 the phosphor layer;
36 a front, transparent set of parallel spaced
37 address lines above the phosphor layer, said front

1 address lines intersecting the rear address lines so as
2 to form pixels at the intersections, said front address
3 lines being separated by laser scribed grooves extending
4 through the underlying phosphor layer and into, but not
5 through, the underlying dielectric layer.

6 88. The EL laminate as set forth in claim 87,
7 wherein the dielectric layer on the rear address lines
8 comprises:

9 a planar layer formed from a ceramic
10 material providing a dielectric strength greater than
11 about 1.0×10^6 V/m and a dielectric constant such that
12 the ratio of the dielectric constant of the dielectric
13 material to that of the phosphor is greater than about
14 50:1, the dielectric layer having a thickness such that
15 the ratio of the thickness of the dielectric layer to
16 that of the phosphor layer is in the range of about 20:1
17 to 500:1, and the dielectric layer having a surface
18 adjacent the phosphor layer which is compatible with the
19 phosphor layer and sufficiently smooth that the phosphor
20 layer illuminates generally uniformly at a given
21 excitation voltage.

22 89. The laminate as set forth in claim 88,
23 wherein the dielectric layer is formed from at least two
24 layers, a first dielectric layer formed on the rear
25 electrode and having a dielectric constant greater than
26 about 500 and a thickness in the range of about 10 to
27 300 microns, and a second dielectric layer formed on the
28 first dielectric layer and having the surface adjacent
29 the phosphor layer as set forth in claim 88, the first
30 and second dielectric layers having a combined thickness
31 of about 10 to 300 microns.

32 90. The laminate as set forth in claim 89,
33 wherein the first and second dielectric layers are
34 formed from ferroelectric ceramic materials having
35 perovskite crystal structures, wherein the first
36 dielectric layer provides a dielectric constant of at
37 least 1000 and has a thickness of about 20 - 150

1 microns, and wherein the second dielectric layer
2 provides a dielectric constant of at least 100 and has
3 a thickness of about 2 - 10 microns.

4 91. The laminate as set forth in claim 90,
5 wherein the first dielectric layer is formed by screen
6 printing and sintering a thick film dielectric paste and
7 the second dielectric layer is formed by sol gel
8 techniques followed by firing.

9 92. The laminate as set forth in claim 91,
10 wherein the first dielectric layer is formed from lead
11 niobate and wherein the second dielectric layer is
12 formed from lead zirconate titanate or lead lanthanum
13 zirconate titanate.

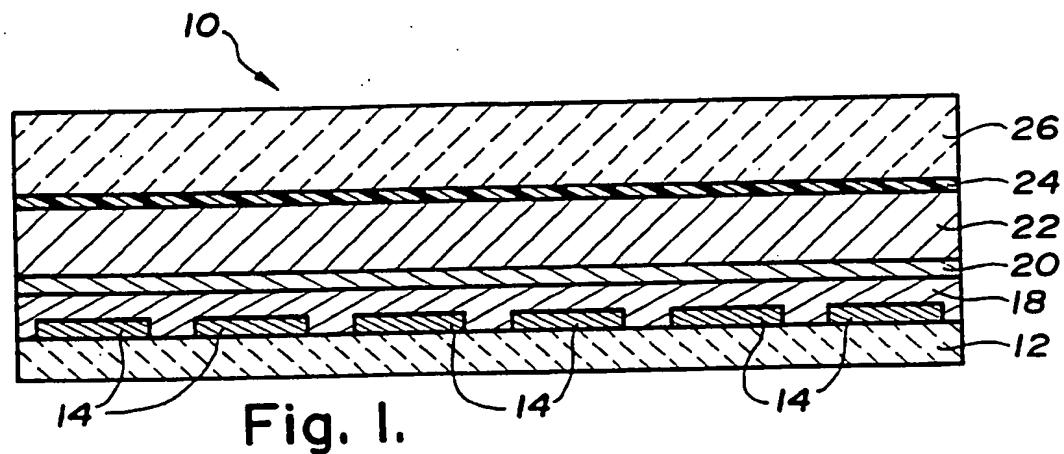


Fig. 1.

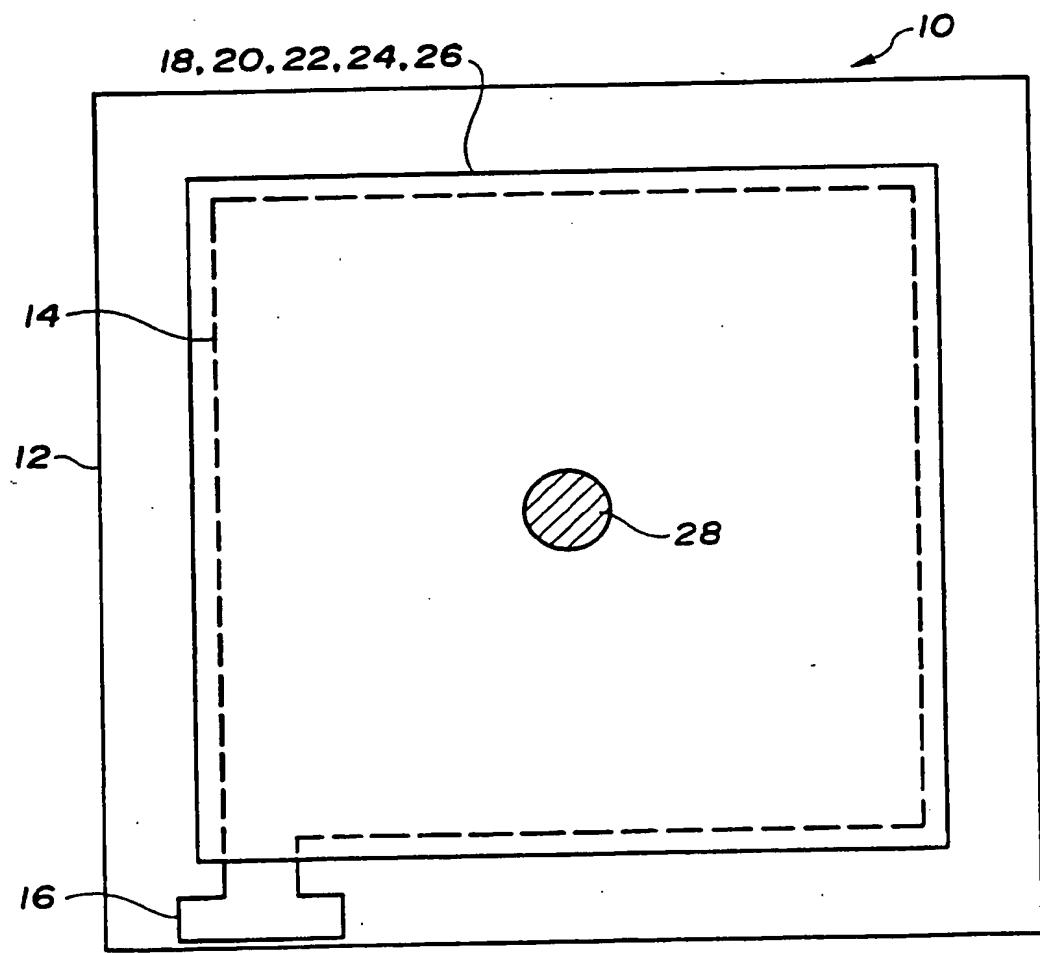


Fig. 2.

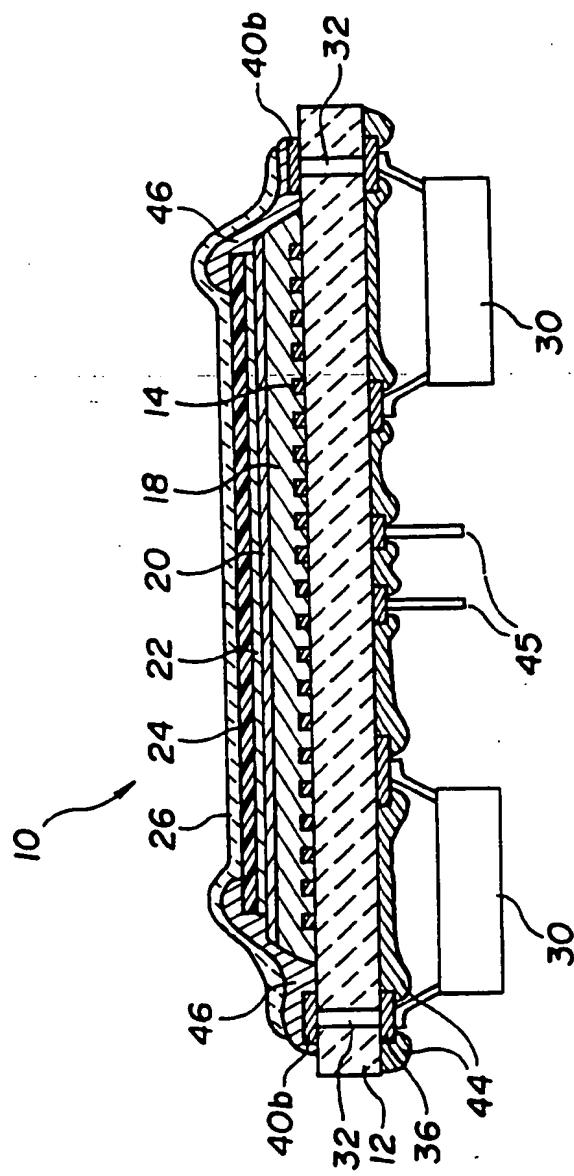


Fig. 3.

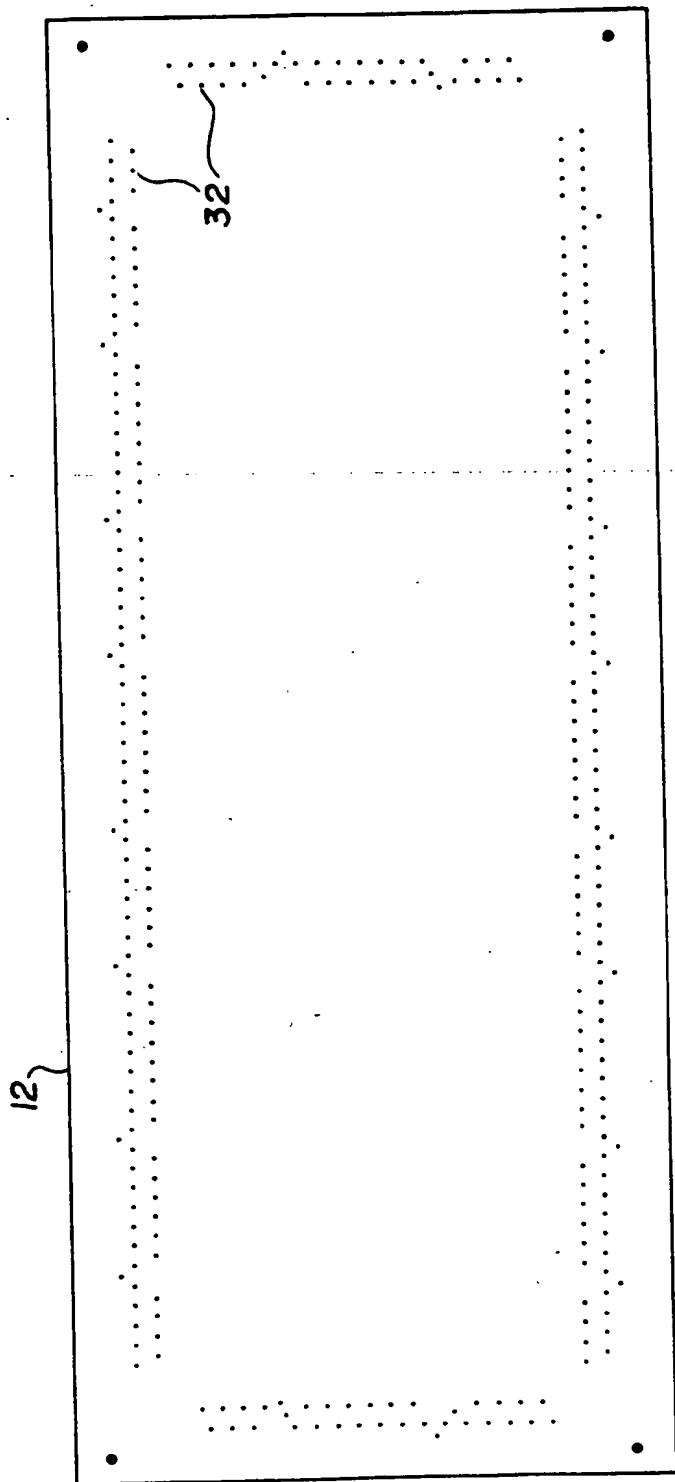


Fig. 4.

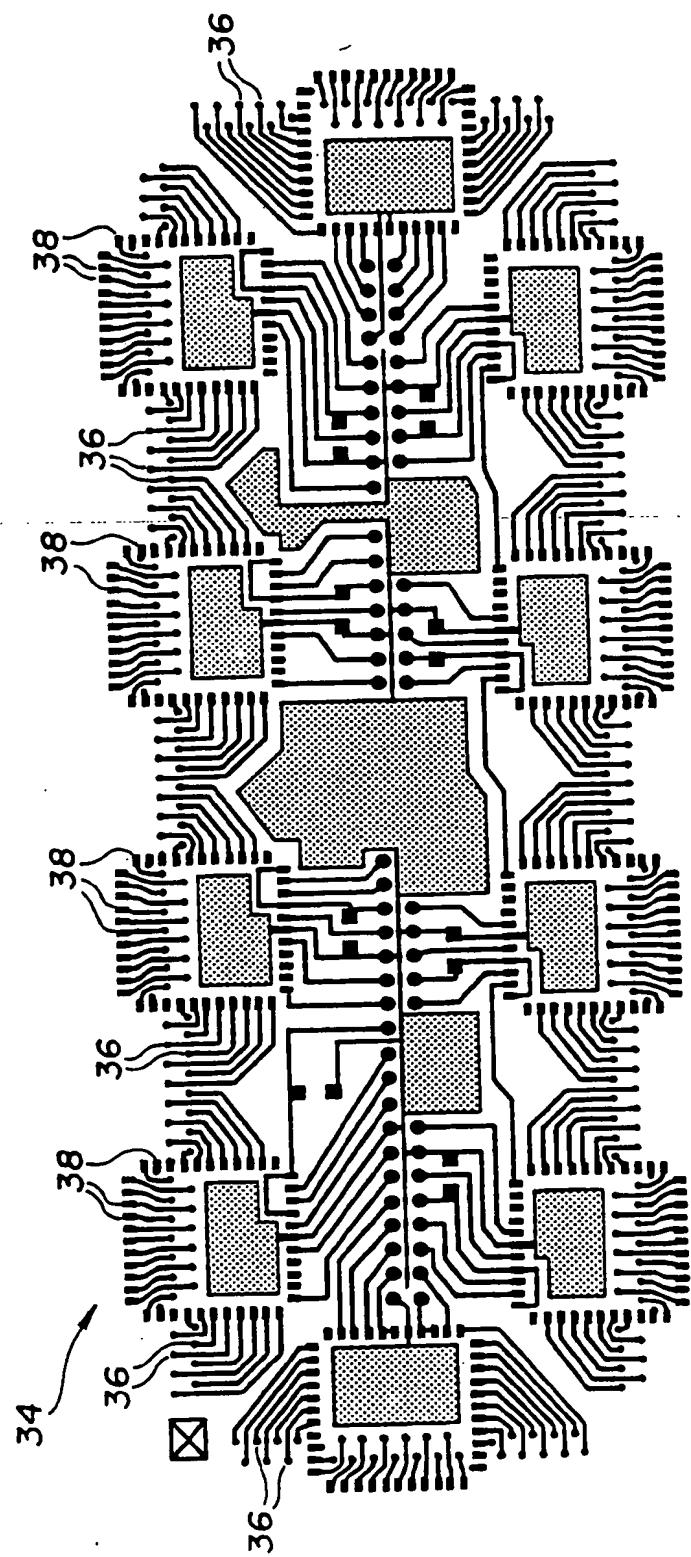


Fig. 5.

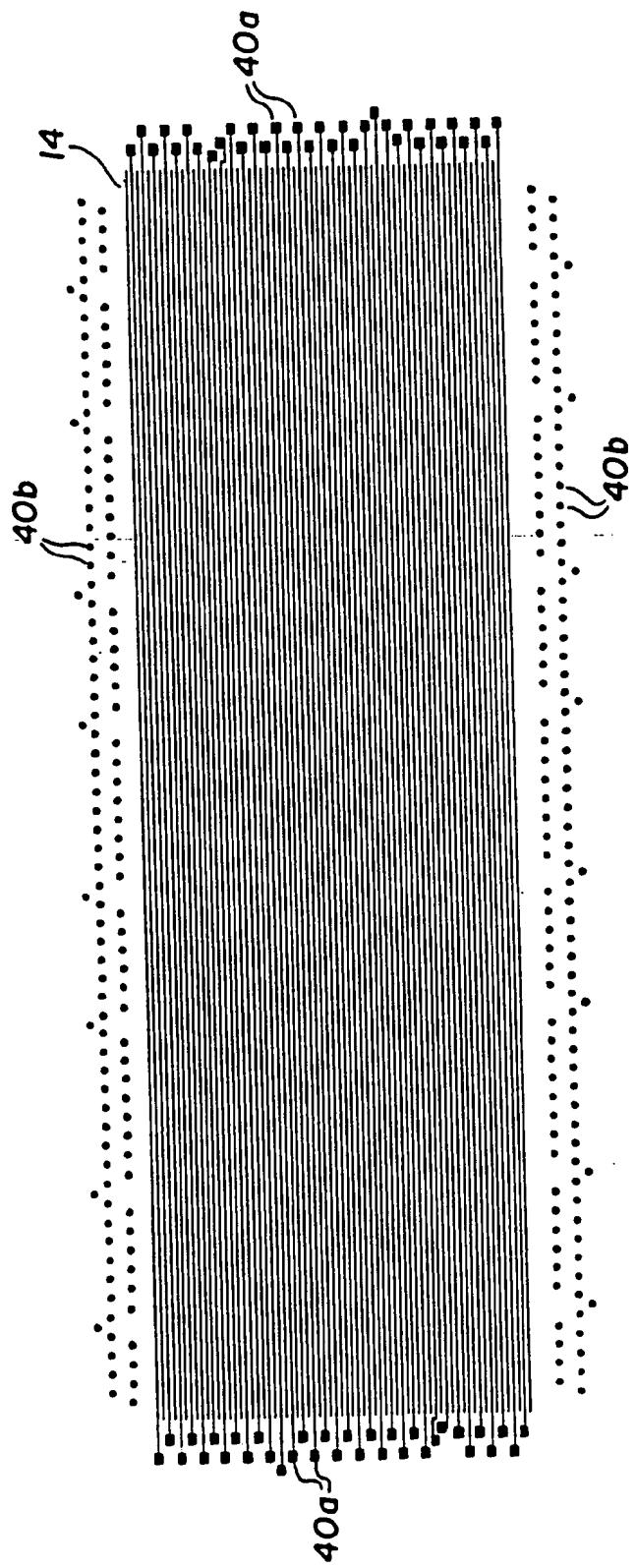


Fig. 6.

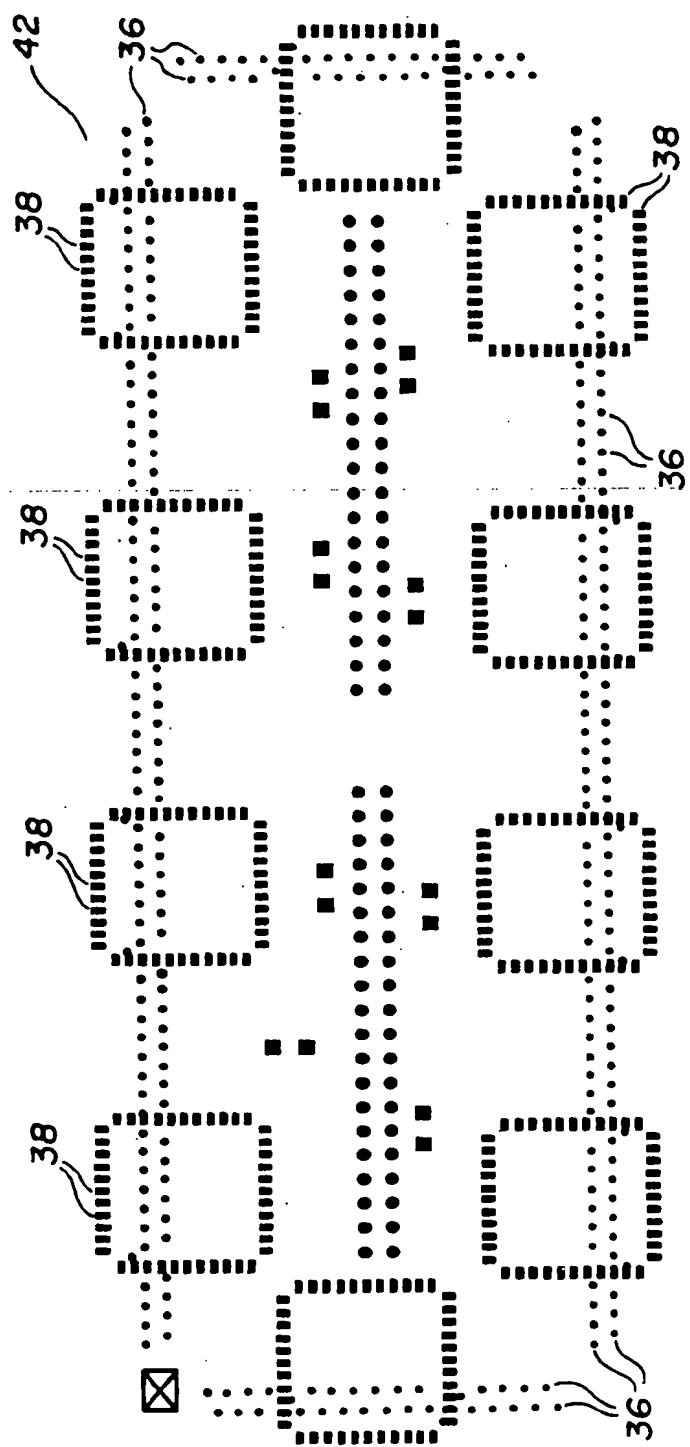


Fig. 7.

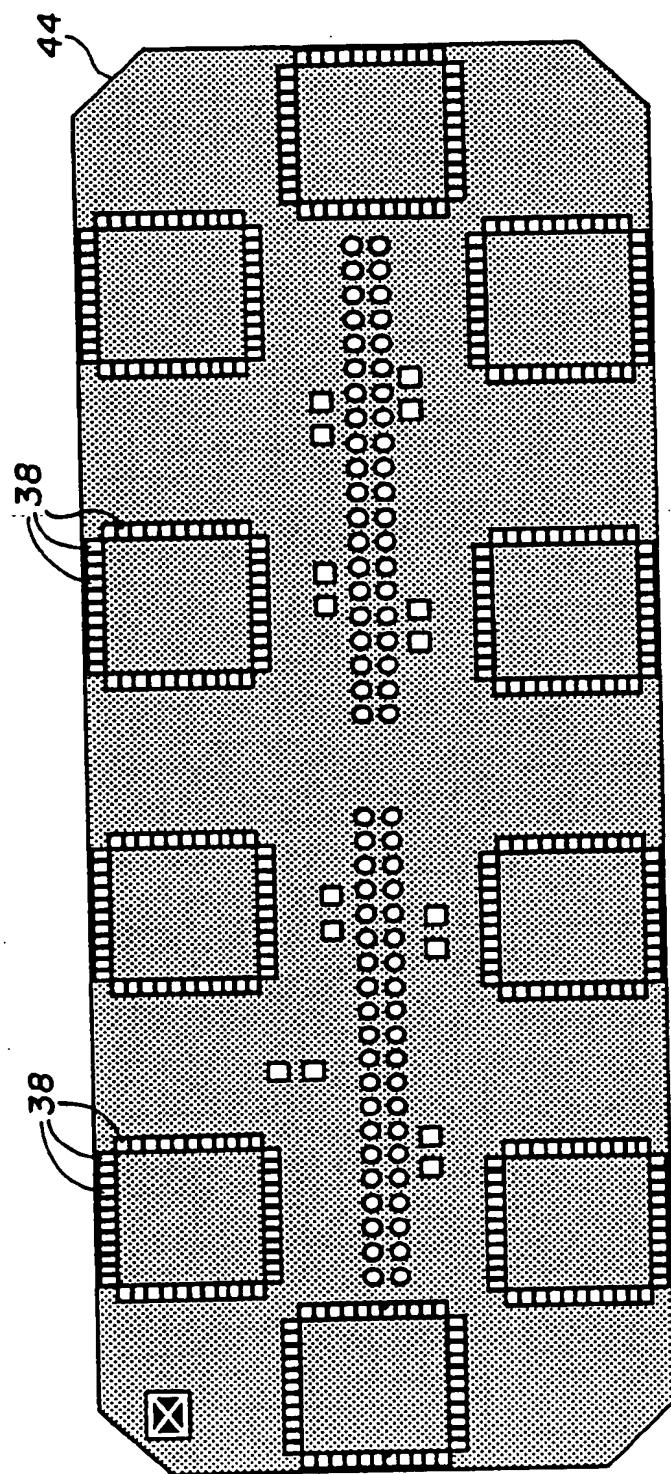


Fig. 8.

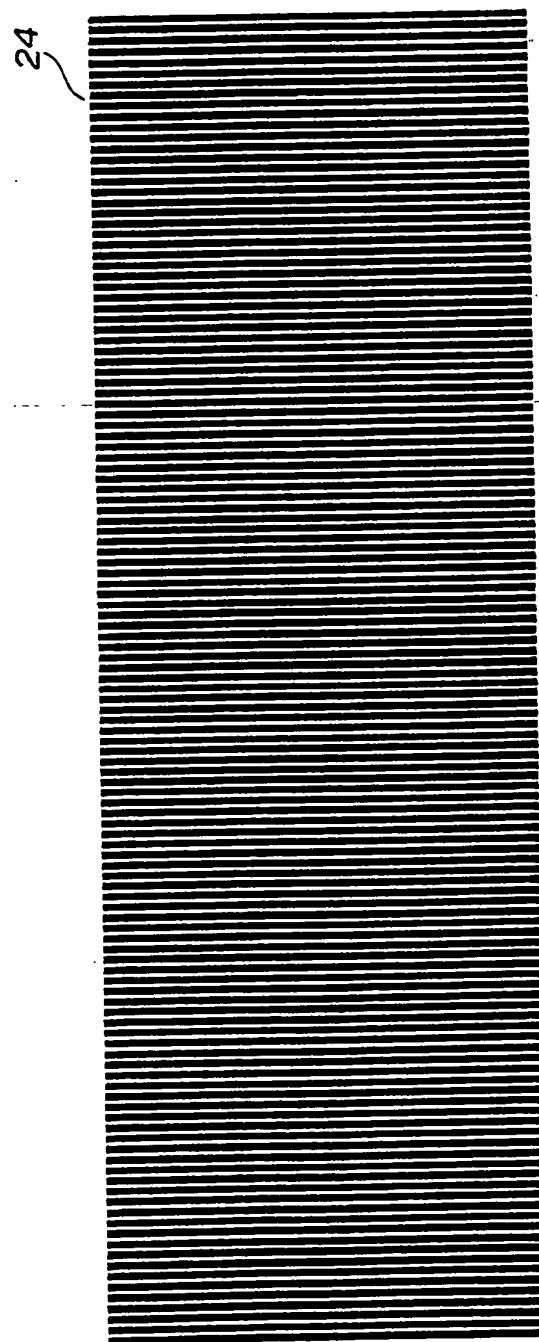


Fig. 9.

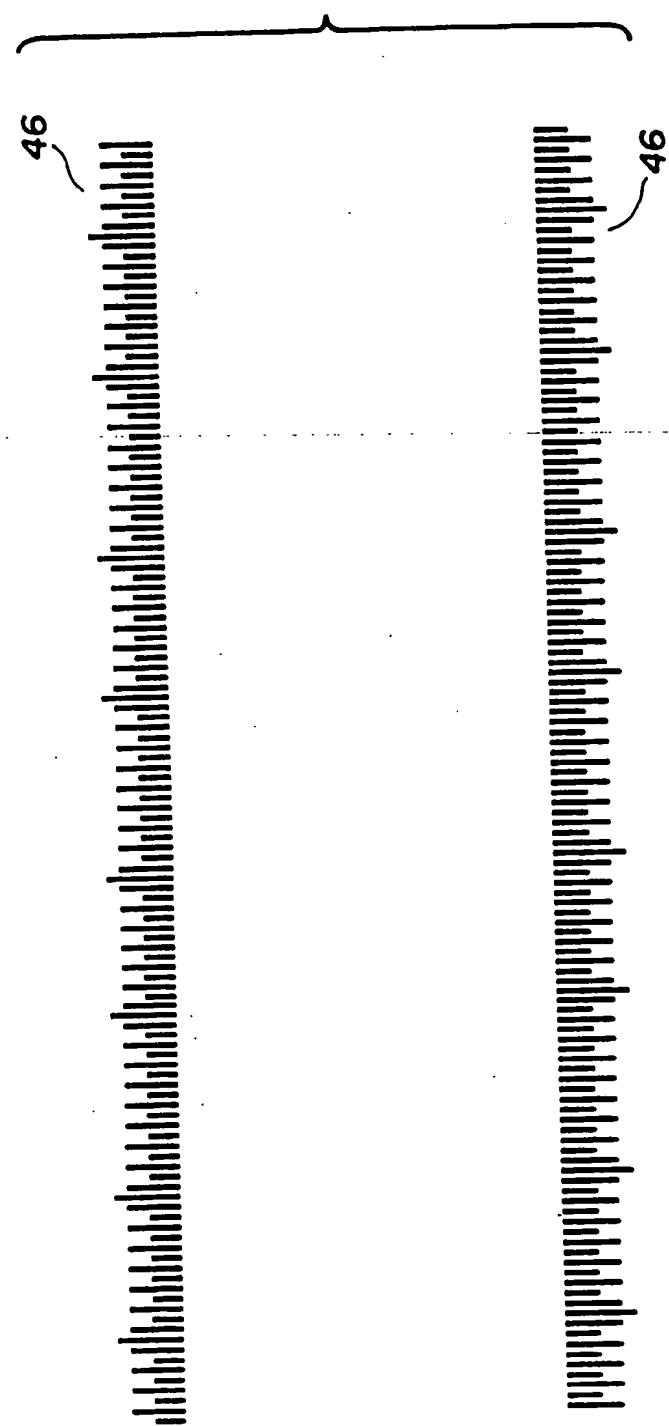


Fig. 10.

INTERNATIONAL SEARCH REPORT

International Application No

PCT/CA 93/00195

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all)⁶

According to International Patent Classification (IPC) or to both National Classification and IPC

Int.C1. 5 H05B33/22; H05B33/10; H05B33/26; H05B33/12

II. FIELDS SEARCHED

Minimum Documentation Searched⁷

| Classification System | Classification Symbols |
|-----------------------|------------------------|
| Int.C1. 5 | H05B |

Documentation Searched other than Minimum Documentation
to the Extent that such Documents are Included in the Fields Searched⁸III. DOCUMENTS CONSIDERED TO BE RELEVANT⁹

| Category ¹⁰ | Citation of Document, ¹¹ with indication, where appropriate, of the relevant passages ¹² | Relevant to Claim No. ¹³ |
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| P,X | US,A,5 131 877 (T.MATHUMOTO) 21 July 1992 see the whole document ---- | 45-57 |
| A | EP,A,0 145 470 (MATSUSHITA) 19 June 1985 see the whole document ---- | 1,3-7, 10,15 |
| A | EP,A,0 111 568 (MATSUSHITA) 27 June 1984 see the whole document ---- | 1,3-7, 10,15 |
| A | US,A,4 857 802 (M.FUYAMA & AL) 15 August 1989 cited in the application see the whole document ---- | 1-3,6,10 --/- |

¹⁰ Special categories of cited documents :¹⁰^{"A"} document defining the general state of the art which is not considered to be of particular relevance^{"E"} earlier document but published on or after the international filing date^{"L"} document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)^{"O"} document referring to an oral disclosure, use, exhibition or other means^{"P"} document published prior to the international filing date but later than the priority date claimed^{"T"} later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention^{"X"} document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step^{"Y"} document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.^{"&"} document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search

06 AUGUST 1993

Date of Mailing of this International Search Report

18.08.93

International Searching Authority

EUROPEAN PATENT OFFICE

Signature of Authorized Officer

DROUOT M.C.

| III. DOCUMENTS CONSIDERED TO BE RELEVANT (CONTINUED FROM THE SECOND SHEET) | | |
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ON INTERNATIONAL PATENT APPLICATION NO.**

CA 9300195
SA 73360

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The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information. 06/08/93

| Patent document cited in search report | Publication date | Patent family member(s) | | Publication date |
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